



Q77H2-AD

Rev : A

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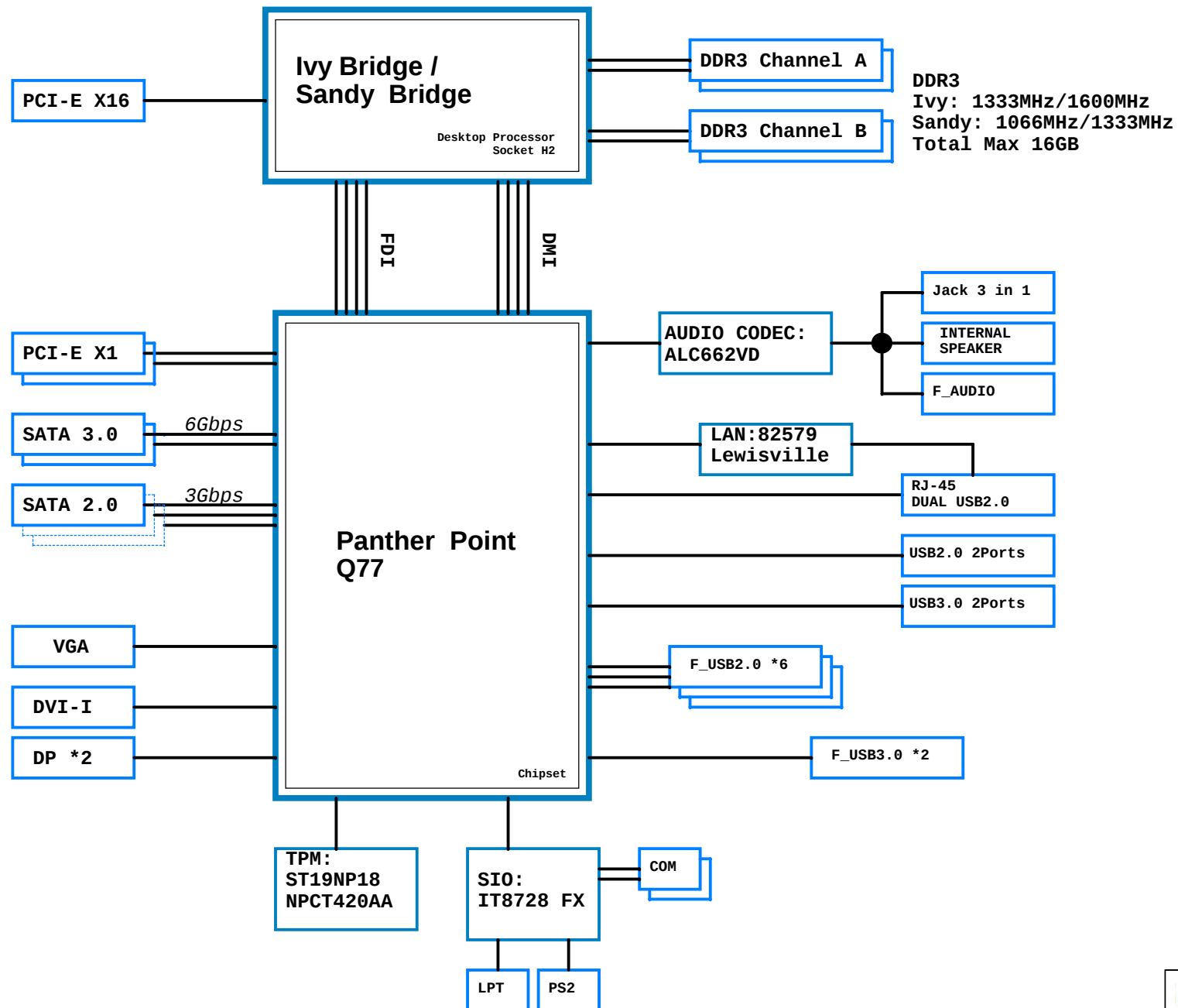
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REVISION HISTORY:

Rev	Date	Notes
V.A	2011/10/03	Initial version

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GPIO Table

PCH

Name	Type	Voltage	Default	Function
GPIO1	I/O	+VCC3	Input	OBR
GPIO6	I/O	+VCC3	Input	Thermal Shut Down
GPIO13	I/O	+3VSB	Input	LPC_PME_L
GPIO15	I/O	+3VSB	Input	TLS_EN
GPIO23	I/O	+VCC3	Input	HDPANEL_DETECT
GPIO28	I/O	+3VSB	Input	ON_DIE_PLL_EN
GPIO45	I/O	+3VSB	Input	SPI_WPSW
GPIO57	I/O	+3VSB	Input	SPI_WP0_L
GPIO59	I/O	+3VSB	Input	LAN_LED_D
GPIO61	I/O	+3VSB	Input	LPCPD_L
GPIO72	I/O	+3VSB	Input	GPIO72_S4SS

IT8728F D/EX

Name	Type	Voltage	Int. Res.	Function
GP14	I/O	+VCC3	OD	Thermal Shut Down
GP15	I/O	+VCC3	OD	MB_ID1
GP16	I/O	+VCC3	OD	PC BEEP
GP22	I/O	+3VSB	OD	LED1
GP23	I/O	+3VSB	OD	LED0
GP35	I/O	+VCC3	OD	MB_ID2
GP36	I/O	+VCC3	OD	GPO36 FOR ACER reserve
GP64	I/O	+VCC3	OD	GPO64 FOR ACER reserve

Strapping Table

PCH Strapping (Page.14)

TLS Confidentiality:

TLS_EN (Internal PD)	
* H	Enable TLS
L	Disable TLS

On-Die PLL VR:

ON_DIE_PLL_EN (Internal PU)	
* H	Enable
L	Disable

Integrated 1.05V SUS VRM:

INTVRMEN	
* H	Enable
L	Disable

No Reboot:

PCH_SPKR (Internal PD)	
* H	Enable No Reboot
L	Disable

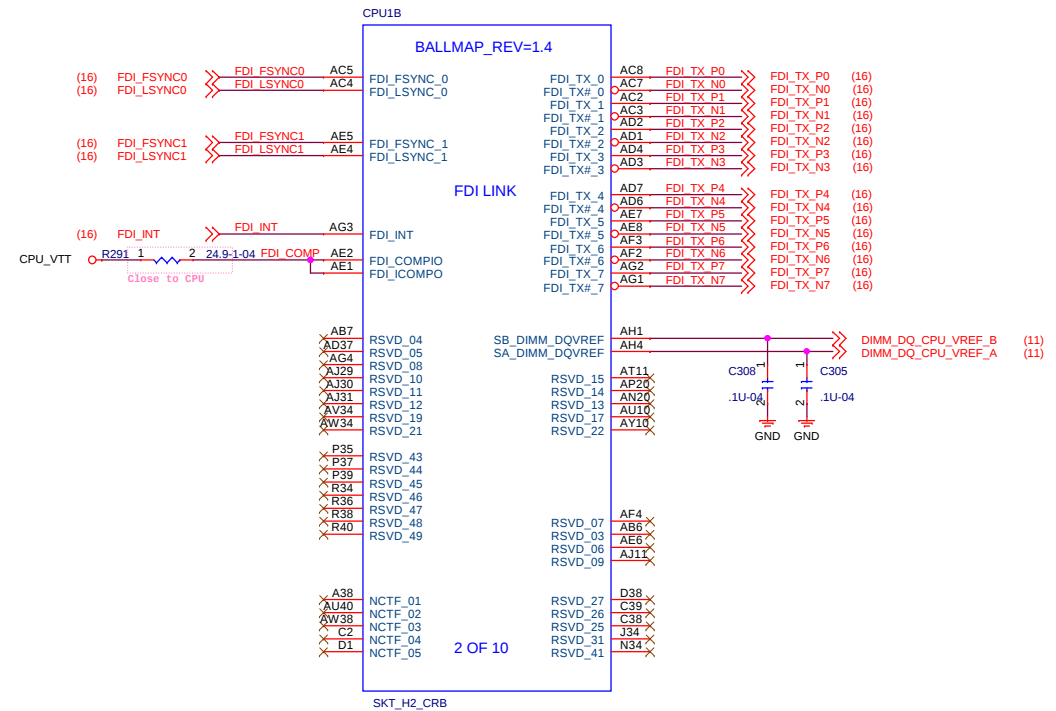
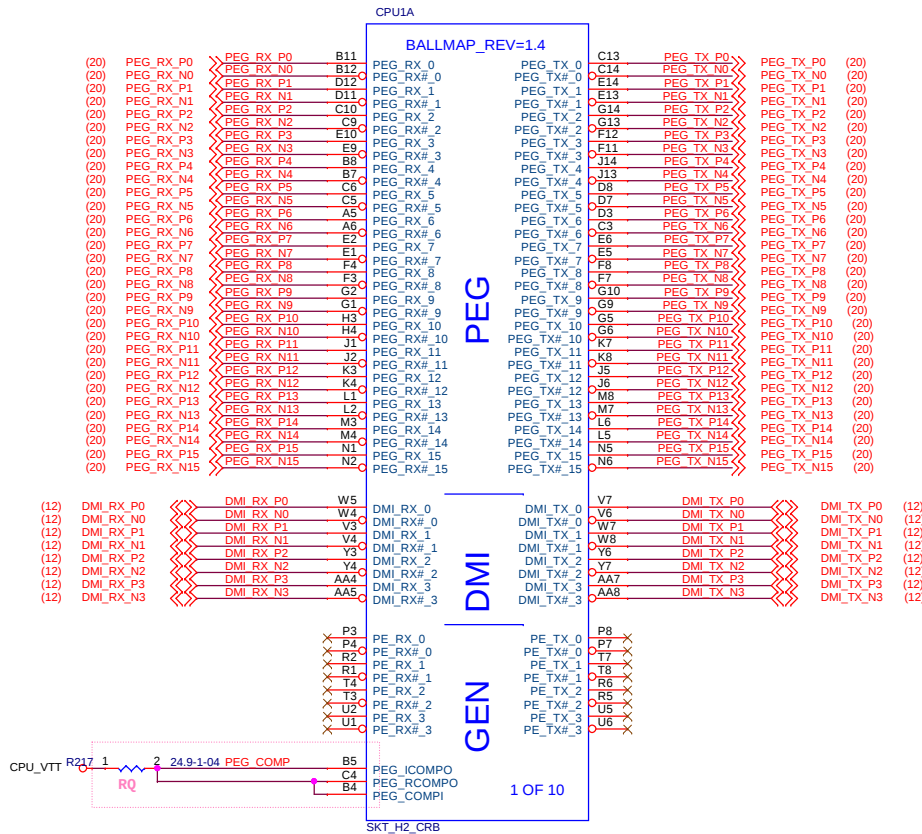
On-Die PLL VR Source:

HDA_SYNC_R (Internal PD)	
H	1.5V
* L	1.8V

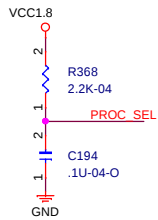
SIO IT8728F D/EX Strapping (Page.28)

Power-On Strapping

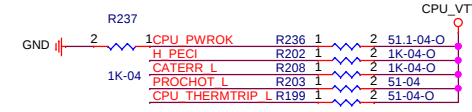
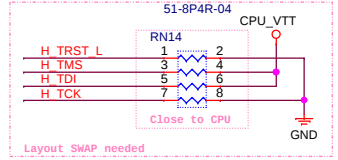
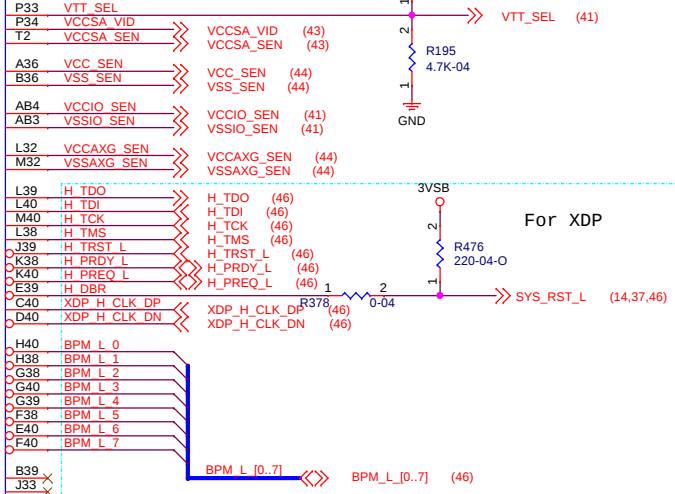
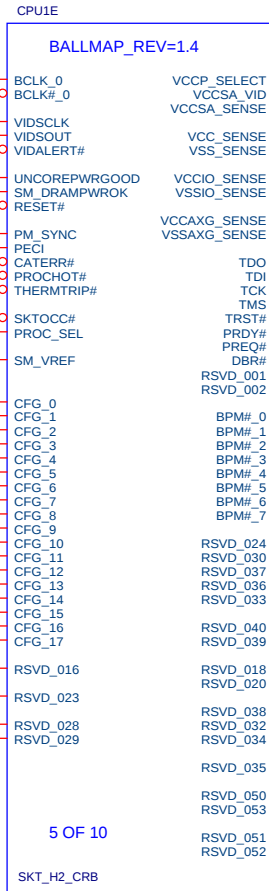
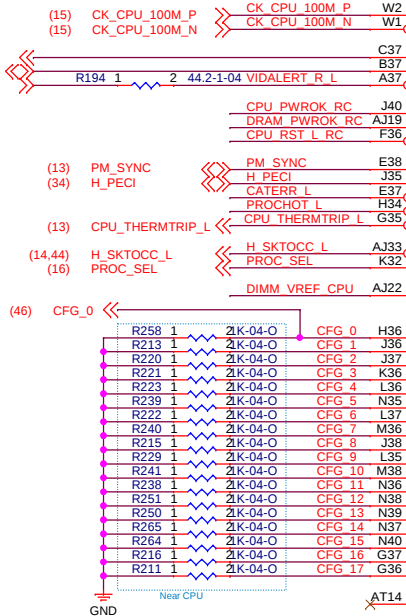
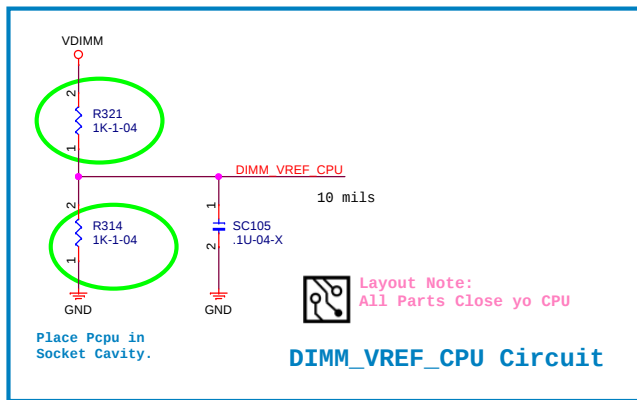
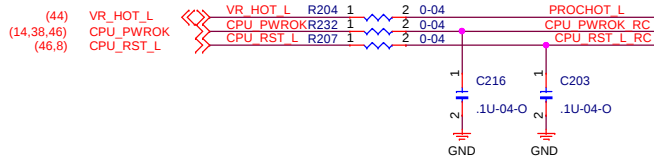
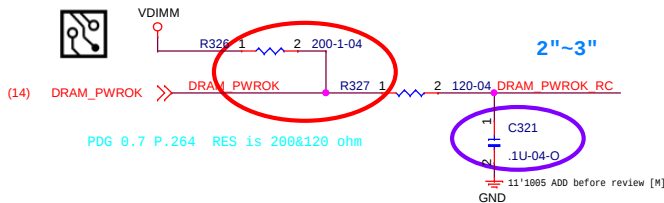
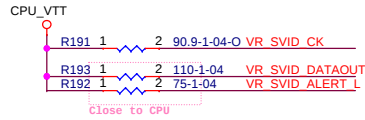
	Symbol	Value	Description
JP1 Pin-48	DSW_EUP_SEL	1	EUP
		0	DSW
JP2 Pin-122	WDT_EN	1	Disable WDT to reset PWR0K
		0	Enable WDT to reset PWR0K
JP3 Pin-124	FAN_CTL_SEL	1	EC Index 63h/6Bh/73h is 80h
		0	EC Index 63h/6Bh/73h is 00h
JP4 Pin-126	K8PWR_EN	1	Disable K8 Power Sequence
		0	Enable K8 Power Sequence
JP5 Pin-29	UOVMODE_SEL	1	Notice Mode (Default)
	OV/UV	0	Force Mode



SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ. 1 ROUTE B5 TO RQ. 1 AS A SEPERATE 12MIL TRACE.



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC IF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	+	+	PEFGSEL[0]
6	+	+	PEFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

PCIE CONFIG	SEL0	SEL1
1x16	1	1
2x8	0	1

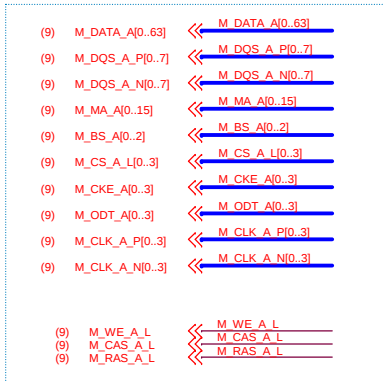
CFG[5:6]:
11=DEFAULT X16,
01=2X8,
10=RESERVED,
00=X8,X4,X4

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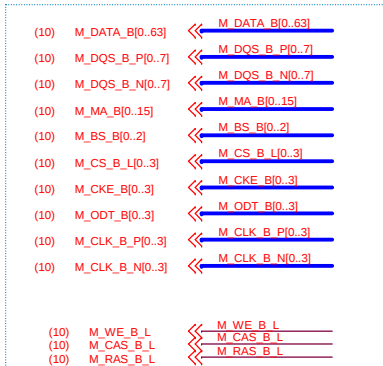
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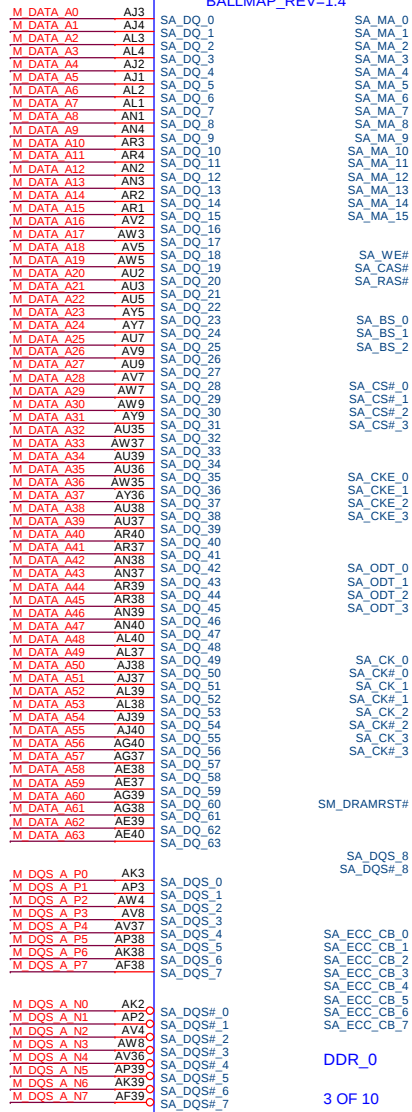
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DDR3 CH. A



DDR3 CH. B



SM_DRAMRST#

SA_DQS_8

SA_ECC_CB_0

SA_ECC_CB_1

SA_ECC_CB_2

SA_ECC_CB_3

SA_ECC_CB_4

SA_ECC_CB_5

SA_ECC_CB_6

SA_ECC_CB_7

SA_ECC_CB_8

SA_ECC_CB_9

SA_ECC_CB_10

SA_ECC_CB_11

SA_ECC_CB_12

SA_ECC_CB_13

SA_ECC_CB_14

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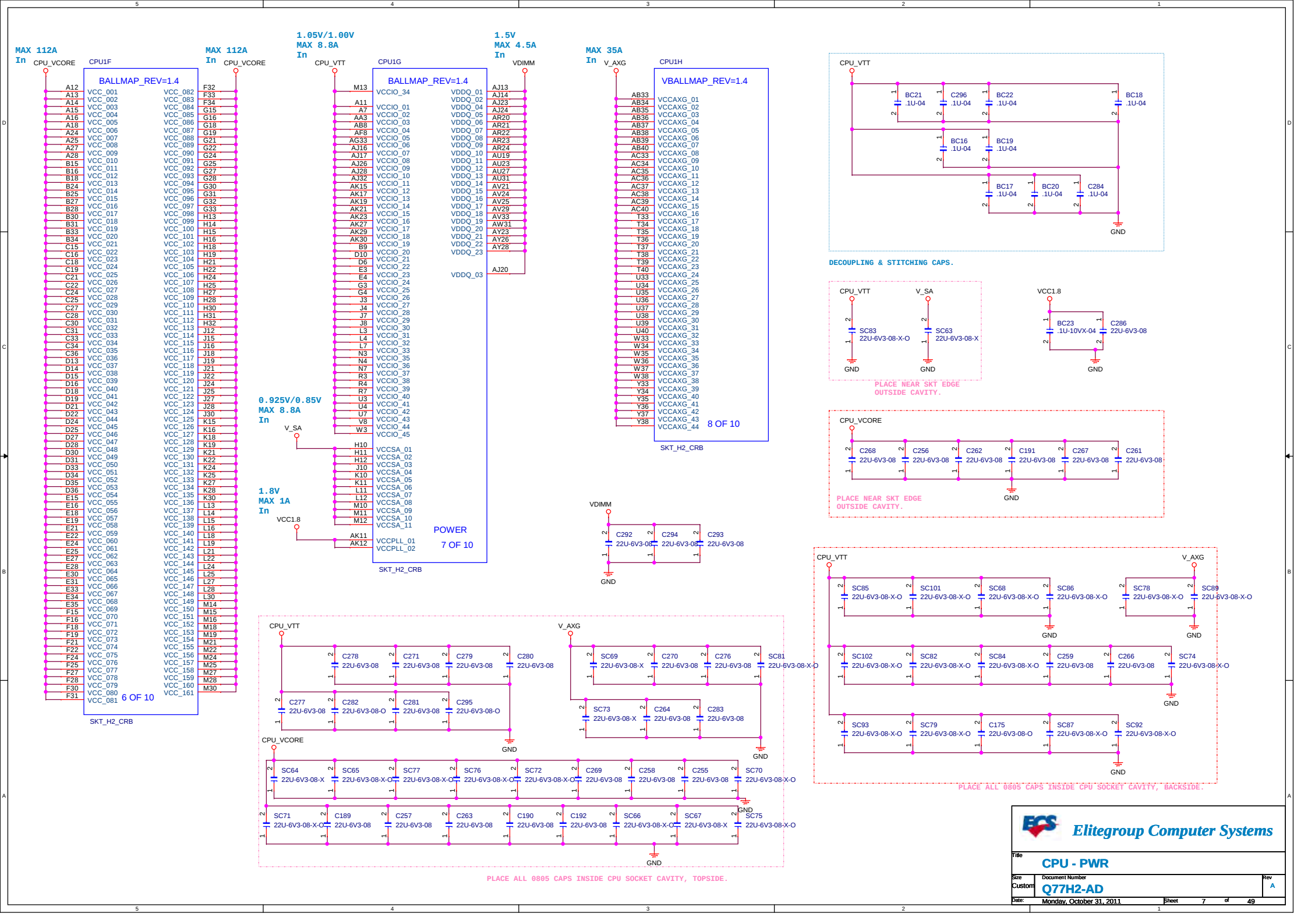
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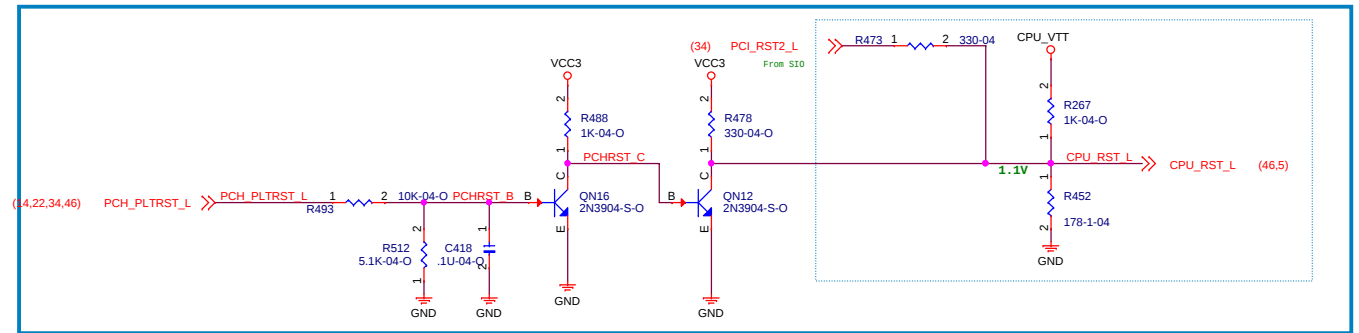
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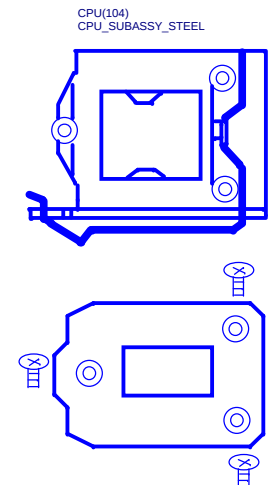
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A17	VSS_001	AM27	AV11	VSS_181	G8
A23	VSS_002	AM3	AV14	VSS_182	H1
A26	VSS_003	AM30	AV17	VSS_183	H17
A29	VSS_004	AM36	AV3	VSS_184	H2
AA35	VSS_005	AM37	AV35	VSS_185	H20
AA33	VSS_006	AM38	AV38	VSS_186	H23
AA34	VSS_007	AM39	AV6	VSS_187	H26
AA35	VSS_008	AM4	AW10	VSS_188	H29
AA36	VSS_009	AM40	AW11	VSS_189	H33
AA37	VSS_010	AM5	AW14	VSS_190	H35
AA38	VSS_011	AN10	AW16	VSS_191	H37
AA6	VSS_012	AN11	AW36	VSS_192	H39
AB5	VSS_013	AN12	AW6	VSS_193	H5
AC1	VSS_014	AN13	AY11	VSS_194	H6
AC6	VSS_015	AN17	AY14	VSS_195	H9
AD33	VSS_016	AN22	AY18	VSS_196	J11
AD36	VSS_017	AN24	AY35	VSS_197	J17
AD38	VSS_018	AN27	AY4	VSS_198	J20
AD39	VSS_019	AN30	AY6	VSS_199	J23
AD40	VSS_020	AN31	AY8	VSS_200	J26
AD5	VSS_021	AN32	B10	VSS_201	J29
AD8	VSS_022	AN33	B13	VSS_202	J32
AE3	VSS_023	AN34	B14	VSS_203	K1
AE33	VSS_024	AN35	B17	VSS_204	K12
AE36	VSS_025	AN36	B23	VSS_205	K13
AF1	VSS_026	AN5	B26	VSS_206	K14
AF34	VSS_027	AN7	B29	VSS_207	K17
AF36	VSS_028	AN8	B32	VSS_208	K2
AF37	VSS_029	AN9	B35	VSS_209	K20
AF40	VSS_030	AP1	B38	VSS_210	K23
AF5	VSS_031	AP11	B6	VSS_211	K26
AF6	VSS_032	AP14	C11	VSS_212	K29
AF7	VSS_033	AP17	C12	VSS_213	K33
AG36	VSS_034	AP22	C17	VSS_214	K35
AH2	VSS_035	AP25	C20	VSS_215	K37
AH3	VSS_036	AP27	C23	VSS_216	K39
AH33	VSS_037	AP30	C26	VSS_217	K5
AH36	VSS_038	AP36	C29	VSS_218	K6
AH37	VSS_039	AP37	C32	VSS_219	L10
AH38	VSS_040	AP4	C35	VSS_220	L17
AH39	VSS_041	AP40	C7	VSS_221	L20
AH40	VSS_042	AP5	C8	VSS_222	L23
AH5	VSS_043	AR11	D17	VSS_223	L26
AH8	VSS_044	AR14	D2	VSS_224	L29
AJ12	VSS_045	AR17	D20	VSS_225	L8
AJ15	VSS_046	AR18	D23	VSS_226	M1
AJ18	VSS_047	AR19	D26	VSS_227	M17
AJ21	VSS_048	AR27	D29	VSS_228	M2
AJ25	VSS_049	AR30	D32	VSS_229	M20
AJ27	VSS_050	AR36	D37	VSS_230	M23
AJ36	VSS_051	AR5	D39	VSS_231	M26
AJ5	VSS_052	AT1	D4	VSS_232	M29
AK1	VSS_053	AT10	D5	VSS_233	M33
AK10	VSS_054	AT12	D9	VSS_234	M35
AK13	VSS_055	AT15	E11	VSS_235	M37
AK14	VSS_056	AT16	E12	VSS_236	M39
AK16	VSS_057	AT17	E17	VSS_237	M5
AK22	VSS_058	AT2	E20	VSS_238	M6
AK28	VSS_059	AT25	E23	VSS_239	M9
AK31	VSS_060	AT27	E26	VSS_240	N8
AK32	VSS_061	AT28	E29	VSS_241	P1
AK33	VSS_062	AT29	E32	VSS_242	P2
AK34	VSS_063	AT3	E36	VSS_243	P36
AK35	VSS_064	AT30	E7	VSS_244	P38
AK36	VSS_065	AT31	E8	VSS_245	P40
AK37	VSS_066	AT32	F1	VSS_246	P5
AK4	VSS_067	AT33	F10	VSS_247	P6
AK40	VSS_068	AT34	F13	VSS_248	R33
AK5	VSS_069	AT35	F14	VSS_249	R35
AK6	VSS_070	AT36	F17	VSS_250	R37
AK7	VSS_071	AT37	F2	VSS_251	R39
AK8	VSS_072	AT38	F20	VSS_252	R8
AK9	VSS_073	AT39	F23	VSS_253	T5
AL11	VSS_074	AT4	F26	VSS_254	T6
AL14	VSS_075	AT40	F29	VSS_255	T8
AL17	VSS_076	AT5	F35	VSS_256	V1
AL19	VSS_077	AT6	F37	VSS_257	V2
AL24	VSS_078	AT7	F39	VSS_258	V33
AL27	VSS_079	AT8	F5	VSS_259	V34
AL30	VSS_080	AT9	F6	VSS_260	V35
AL36	VSS_081	AT9	F9	VSS_261	V36
AL5	VSS_082	AU1	G11	VSS_262	V37
AM1	VSS_083	AU15	G12	VSS_263	V38
AM11	VSS_084	AU16	G17	VSS_264	V39
AM14	VSS_085	AU26	G20	VSS_265	V40
AM17	VSS_086	AU34	G23	VSS_266	V5
AM2	VSS_087	AU4	G26	VSS_267	V6
AM21	VSS_088	AU6	G29	VSS_268	V8
AM23	VSS_089	AV10	G34	VSS_269	Y5
AM25	VSS_090		G7	VSS_270	Y8
A4	VSS_NCTF_01		AY37	VSS_NCTF_03	
AV39	VSS_NCTF_02		B3	VSS_NCTF_04	

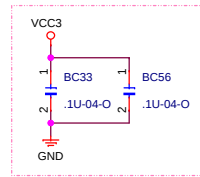
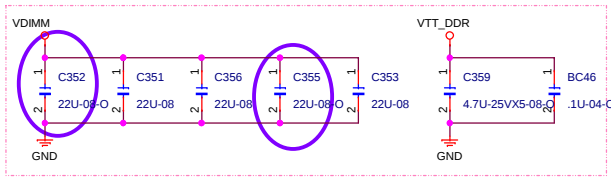
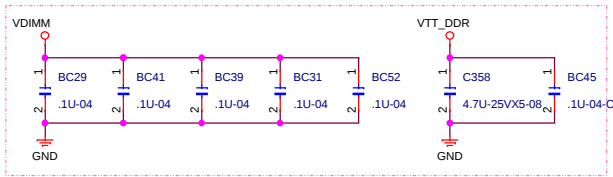
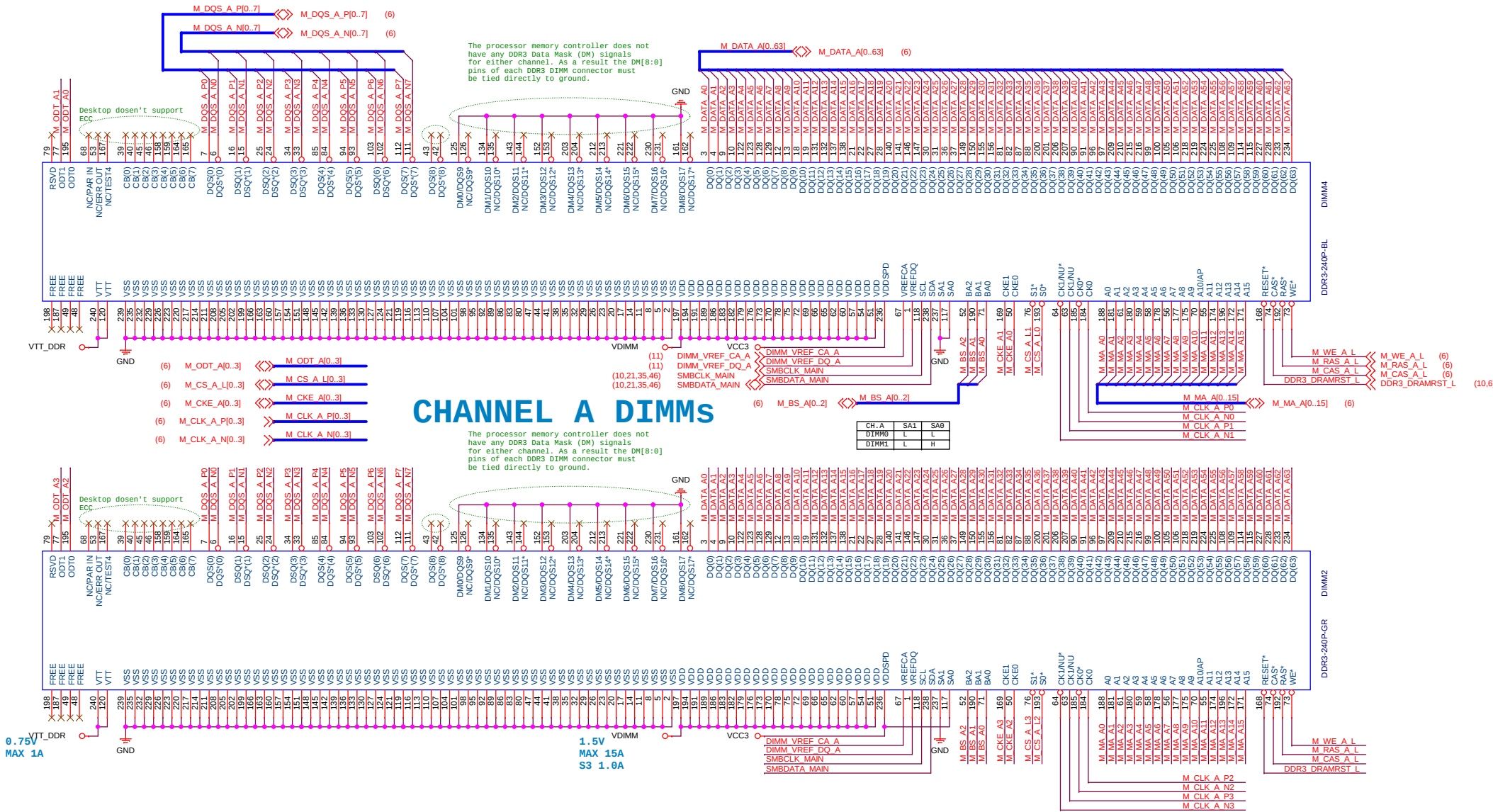


PLTRST_L Driving Circuit

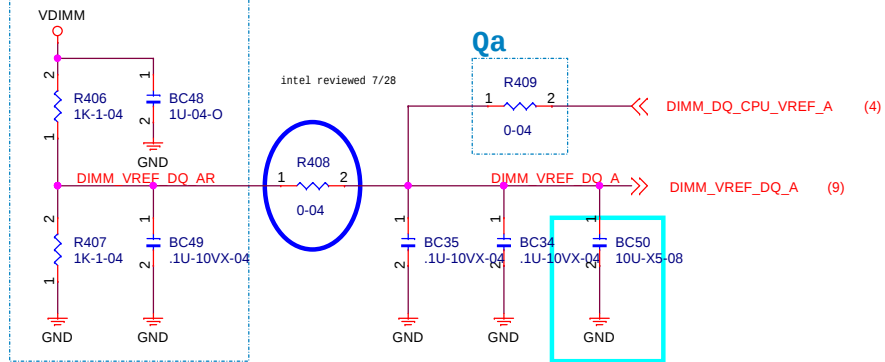
11-010-115123 CPU SMD SOCKET
SOCKET.CPU..LGA 1155P SMD..6/F...BLACK.
ACA-ZIF-096-E02...LEAD-FREE(RoHS/HF)...L0TES

20-800-005011 SUBASSY.STEEL....LGA 1155P....
W/BACK PLATE.ACA-ZIF-082-E23...LEAD-FREE(RoHS)...L0TES



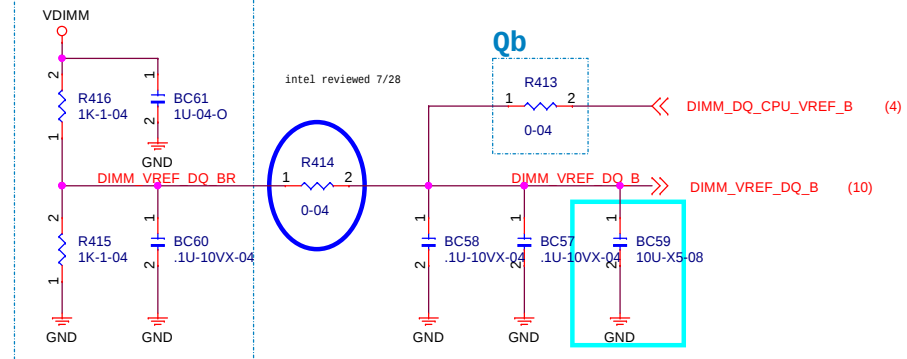


Pa

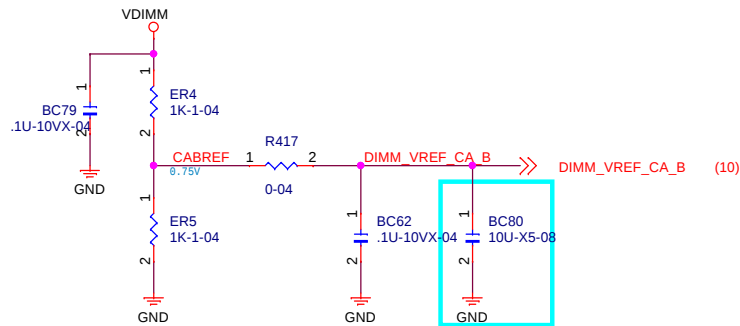
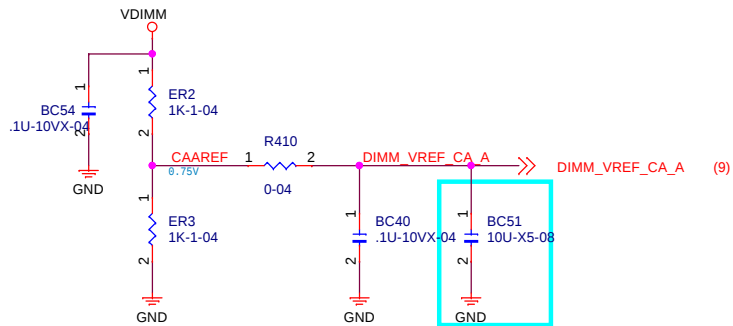


Layout Note:
All parts close to DDR3 Slots.

Pb



DIMM_VREF_DQ Control Circuit

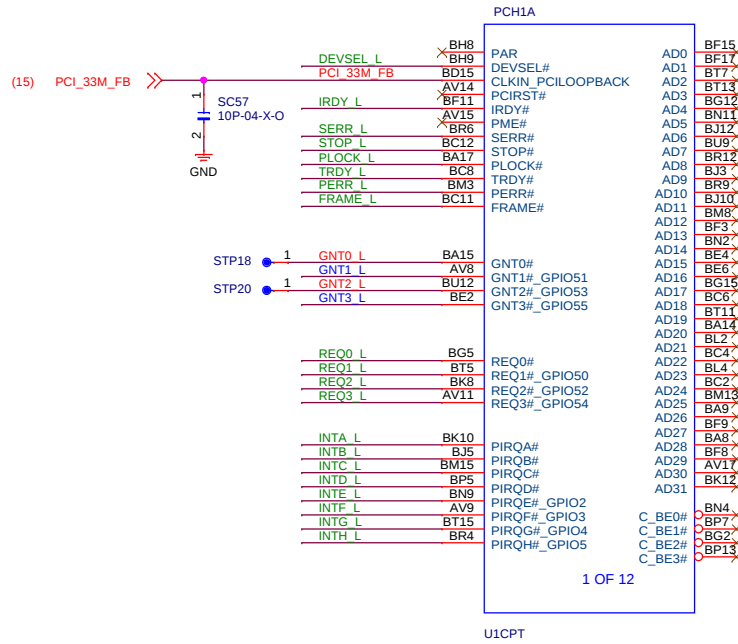


DIMM_VREF_CA Circuit



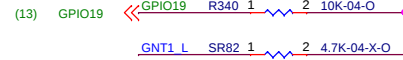
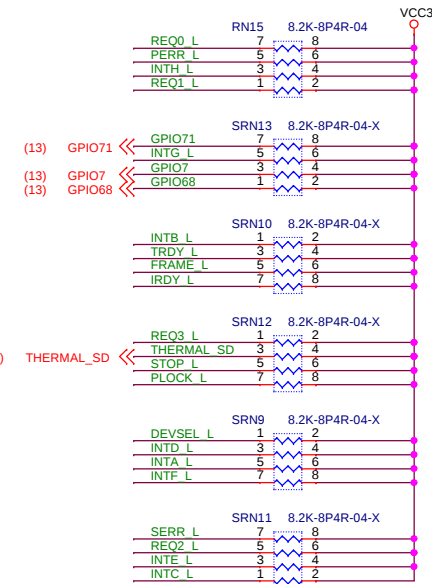
Elitegroup Computer Systems

Title		
DDR3 - VREF		
Size	Document Number	Rev
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PCI-E X1

Giga Lan

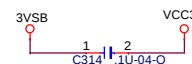
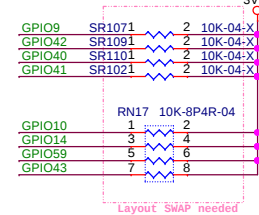
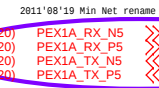


Boot Device Select:

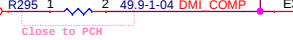
BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

*

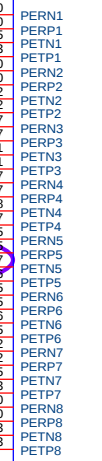
GNT[0..3]# have been internal pull high to +VCC3

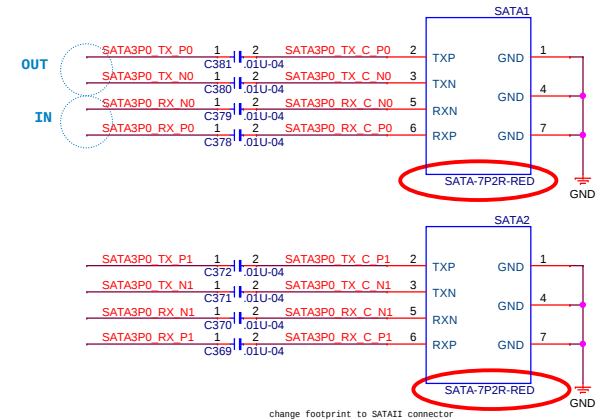
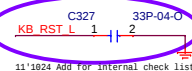
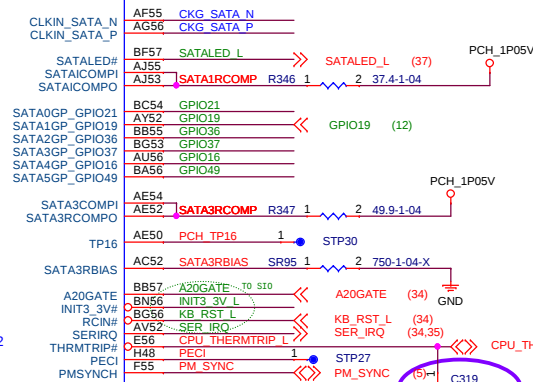
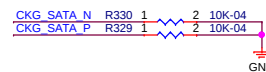
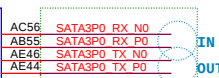
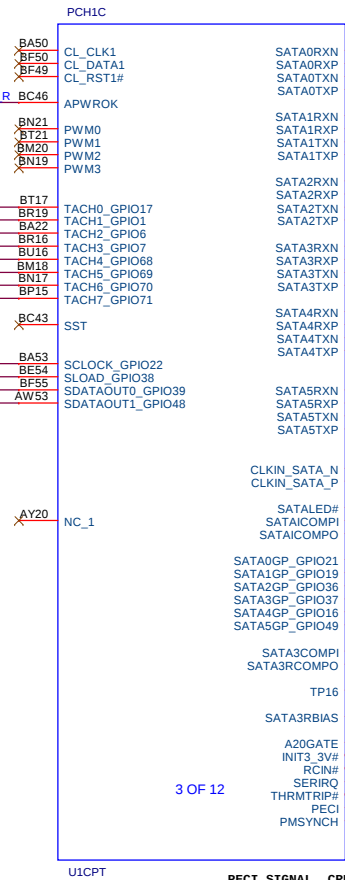
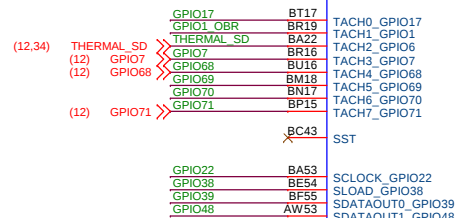
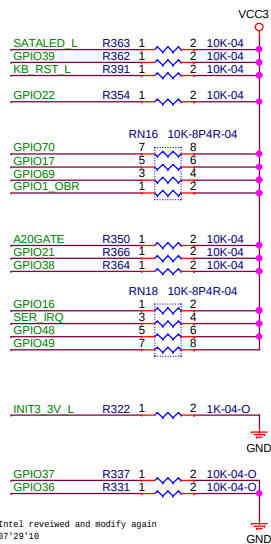
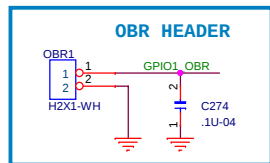
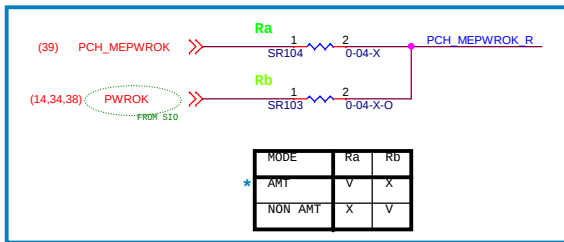


PCH1P05V



PCH1B

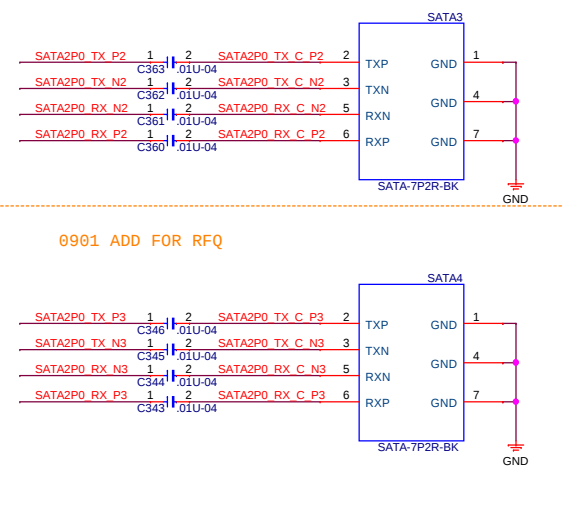




Layout Note:

SATA3.0 4.5/7.5/20 in 90 Q ±17.5%

SATA2.0 4.5/7.5/15 in 90 Q ±17.5%

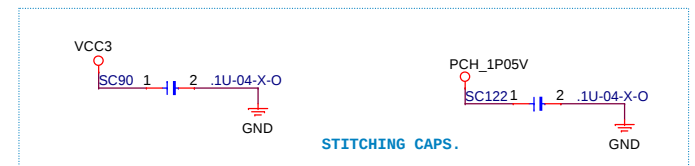
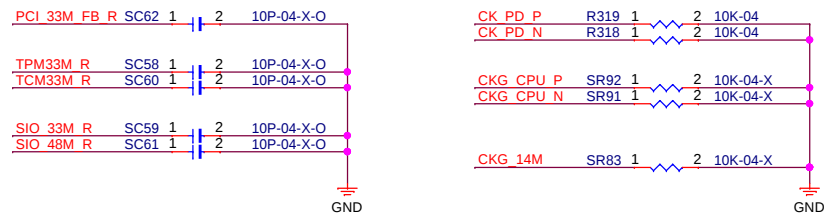
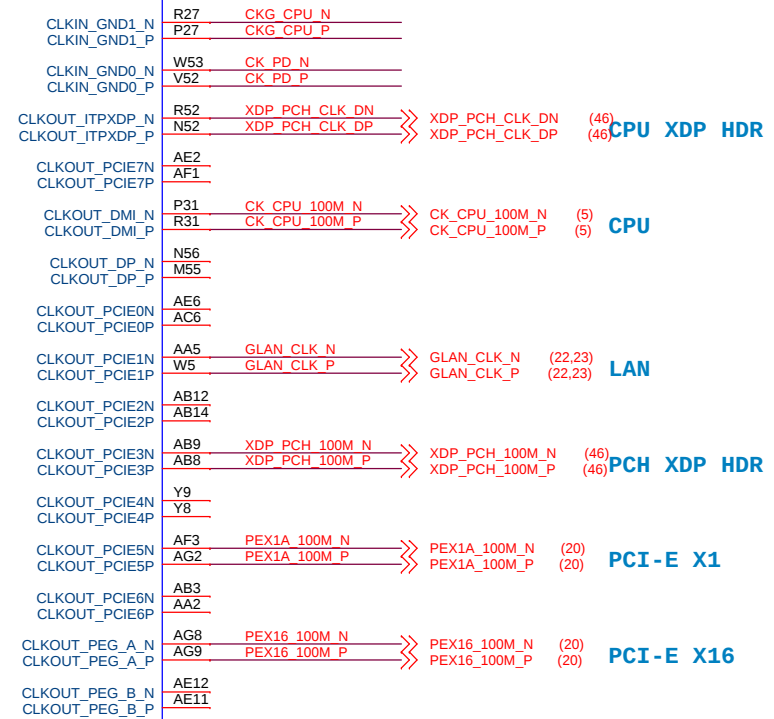
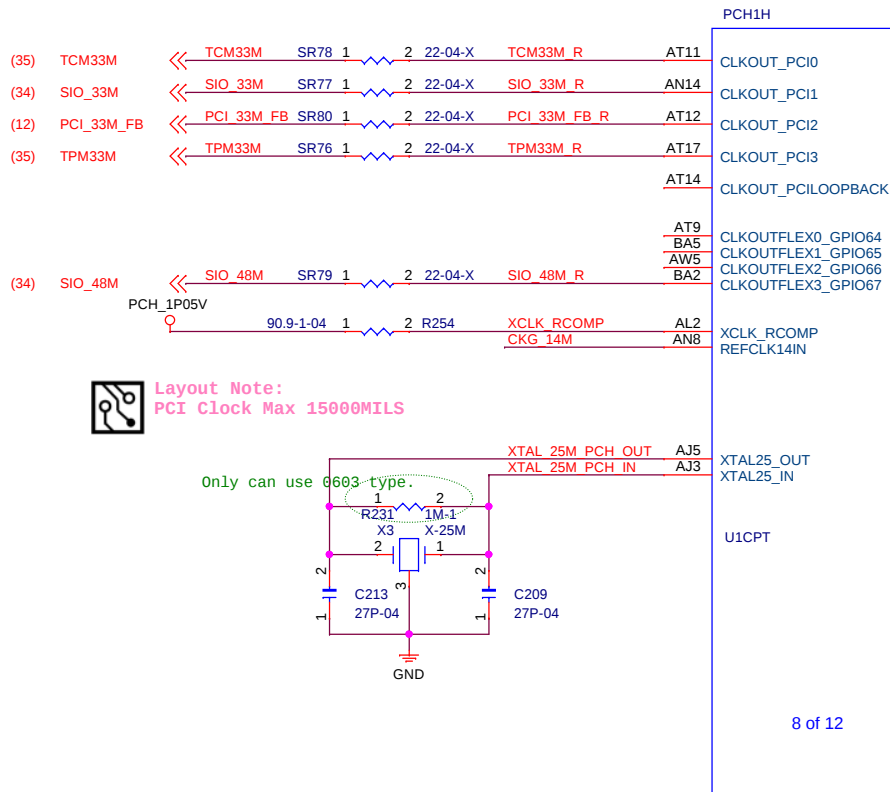


Elitegroup Computer Systems

Title PCH - SATA, SATA CONN, OBR

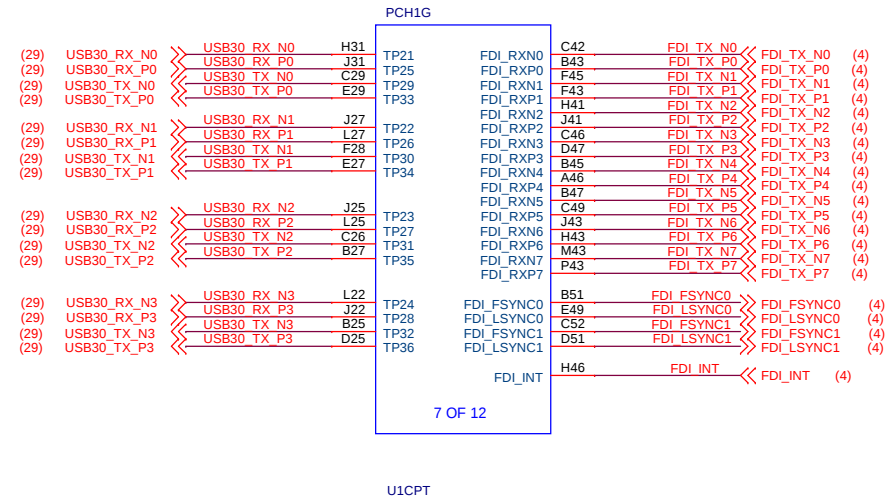
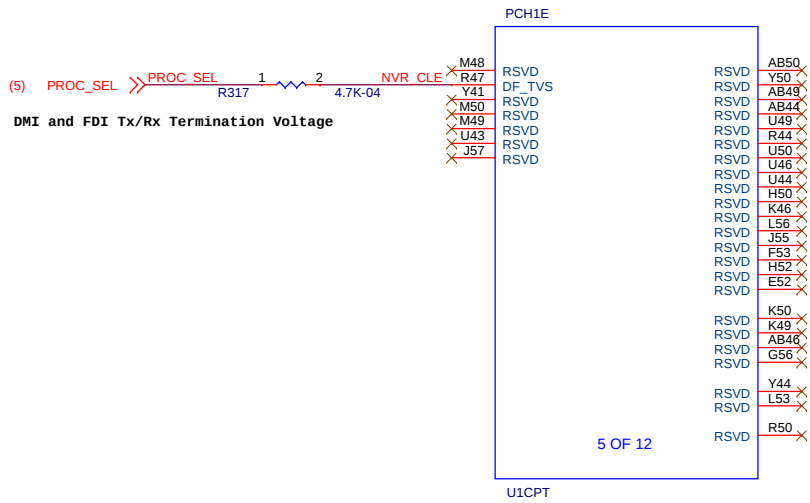
Size Custom Document Number Q77H2-AD Rev A

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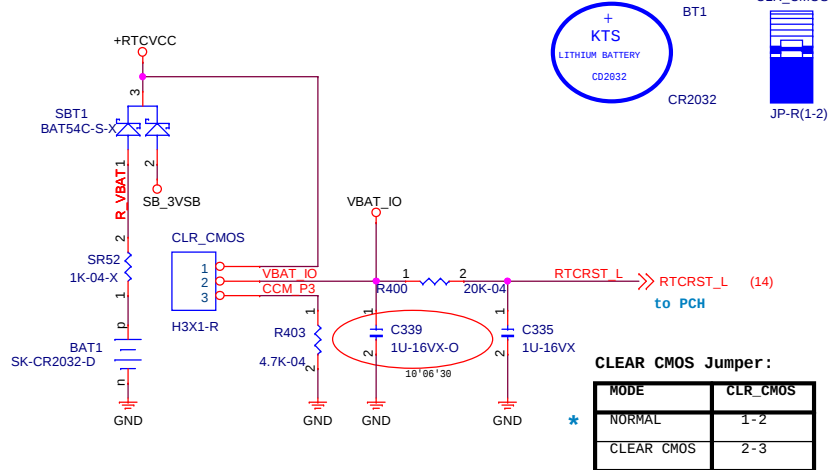


ECS Elitegroup Computer Systems

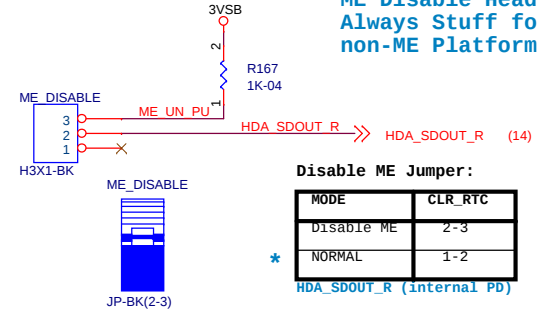
Title		
PCH - CLK IO		
Size	Document Number	Rev
Custom	Q77H2-AD	A
Date:	Monday, October 31, 2011	Sheet 15 of 49



CLR_CMOS



ME Disable Header, Always Stuff for ME or non-ME Platform.



Elitegroup Computer Systems

Title		
PCH - USB3.0/FDI, CLR_CMOS		
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Port-B: DVI

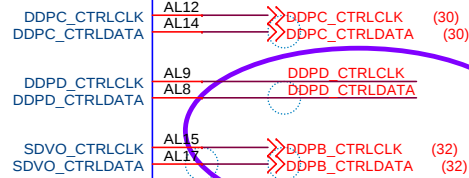
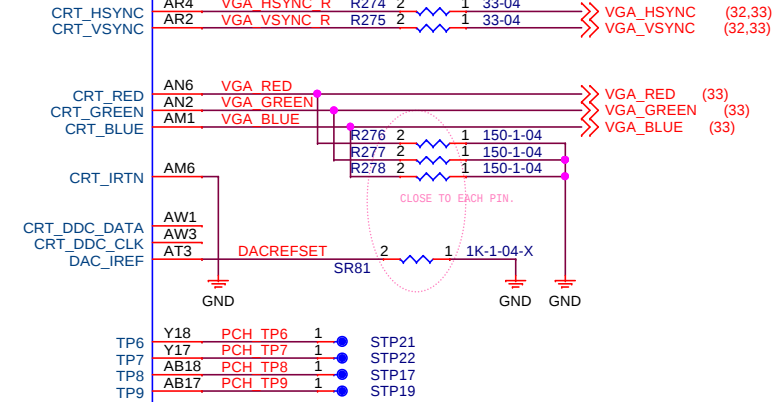
Port-C: DP

Port-D: DP

[M 1007] PORTB CHANGE TO CONNECT TO DVI-I
PORT D CHANGE TO CONNECT TO DP

PCH1F

U1CPT

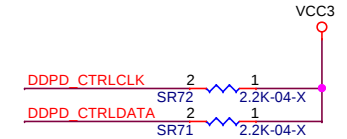
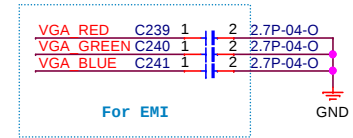


6 of 12

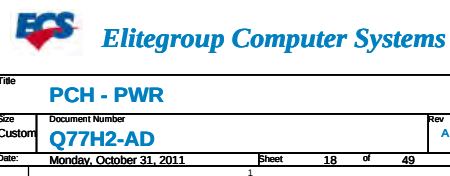
Port C Detected(Internal PD):
Port C is Detected when High,
Port C is not Detect when Low.

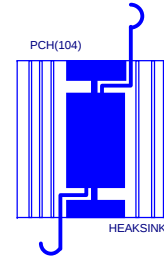
Port D Detected(Internal PD):
Port D is Detected when High,
Port D is not Detect when Low.

Port B Detected(Internal PD):
Port B is Detected when High,
Port B is not Detect when Low.

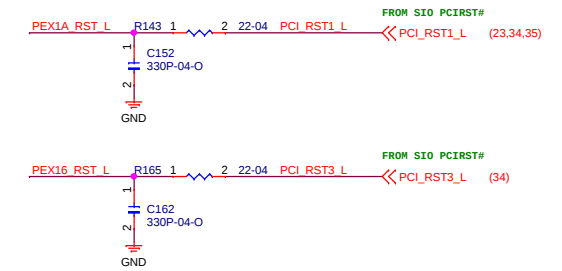
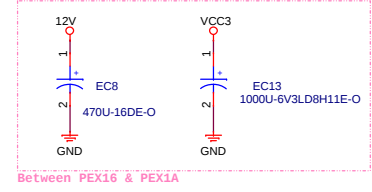
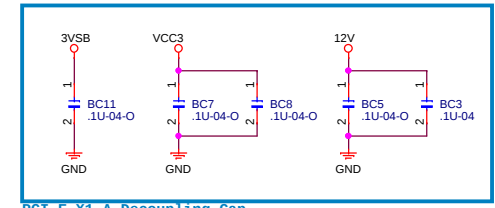
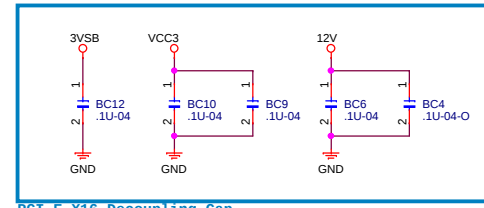
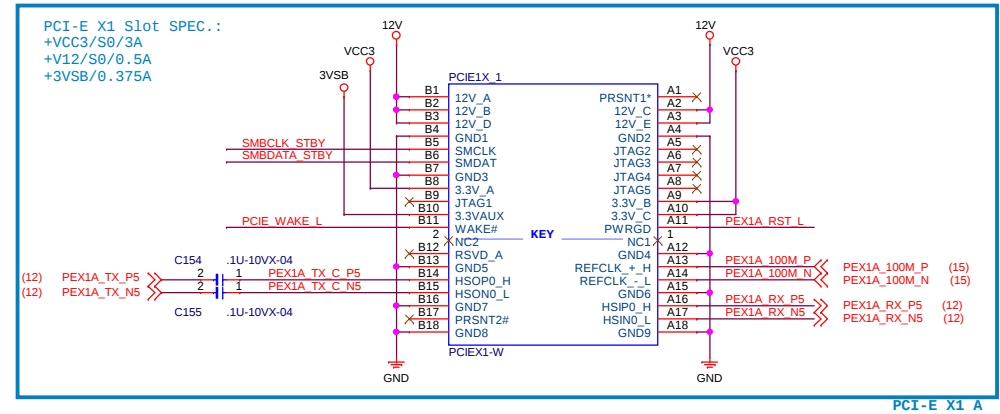


Title			PCH - DISPLAY/VGA
Size	Document Number	Rev	A
Custom	Q77H2-AD		
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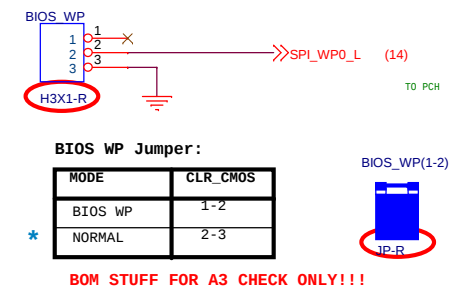
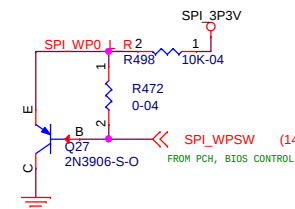
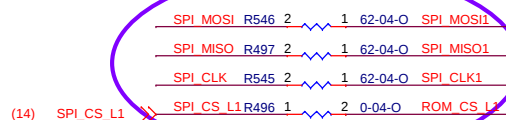
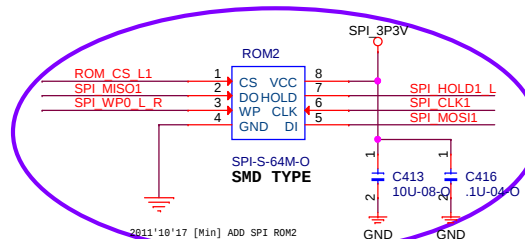
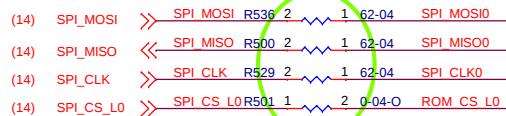
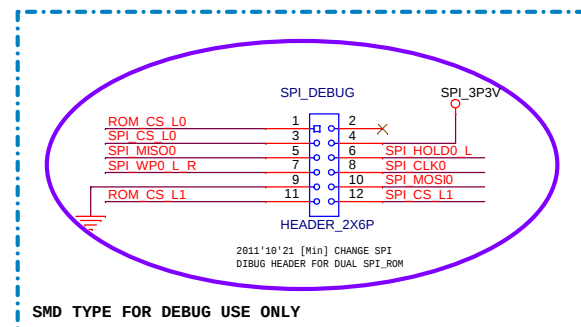
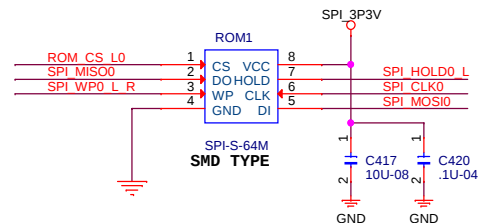
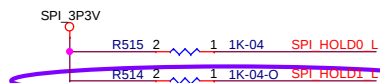
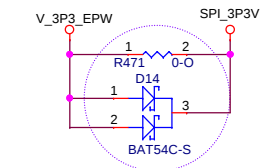




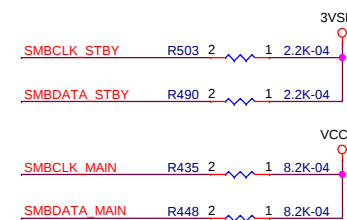
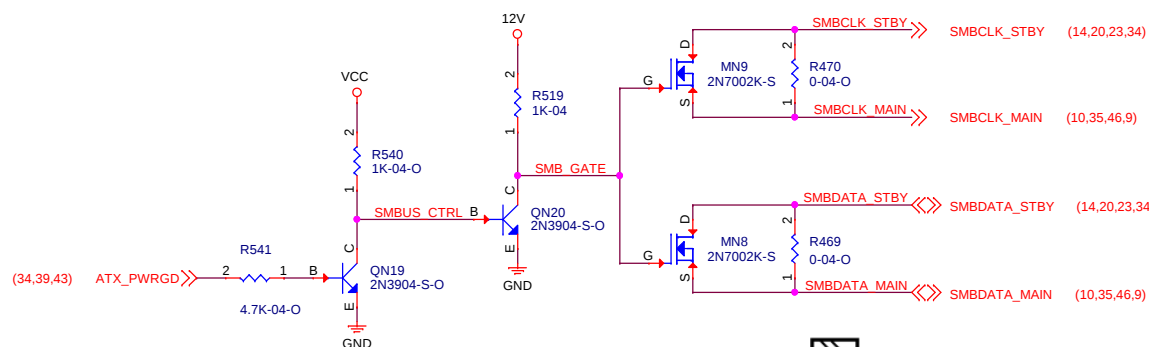
PCI-E X16 Slot SPEC.:
 +VCC3/S0/3A
 +V12/S0/5.5A
 +3VSB/0.375A



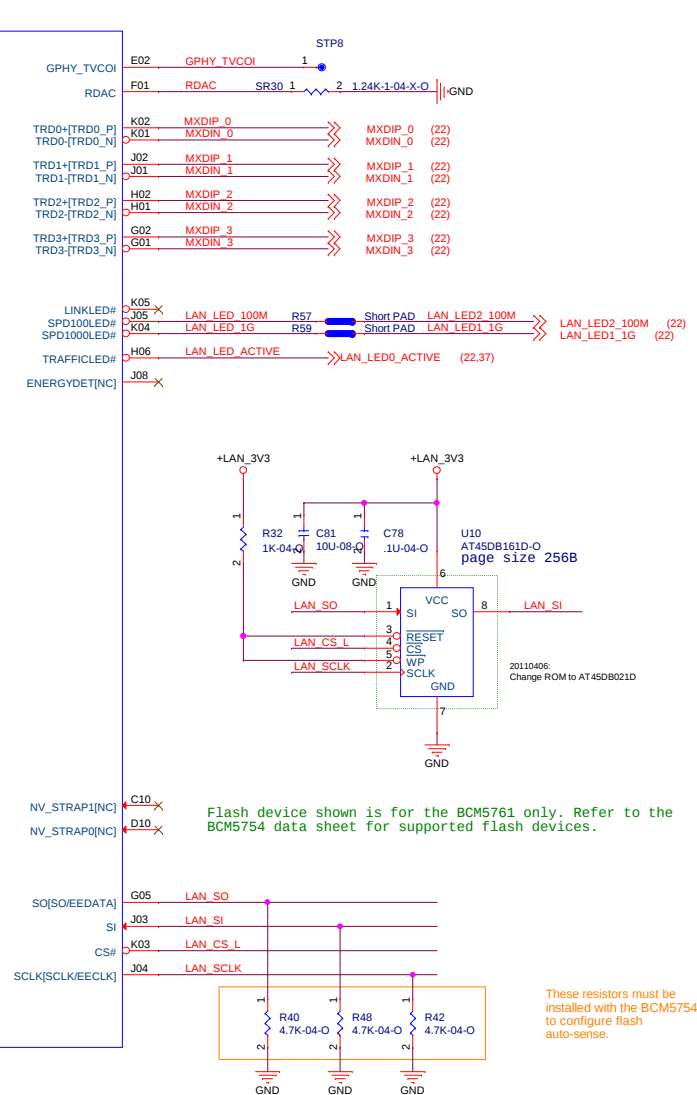
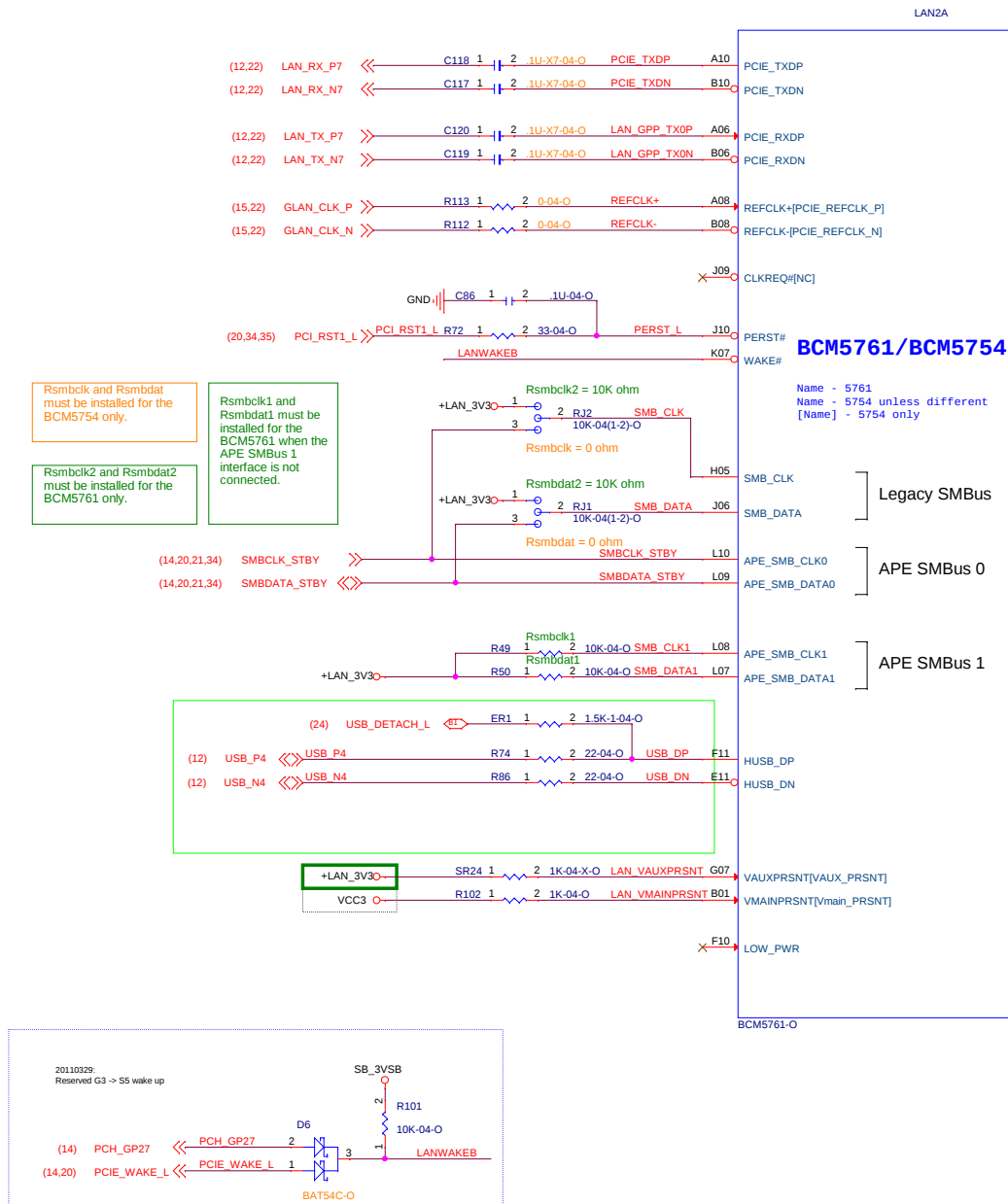
SPI ROM Circuit



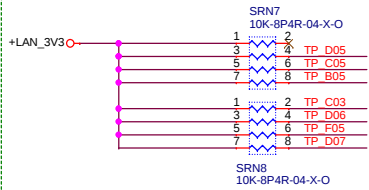
SMBUS Logic Circuit



Layout Note:
SMBUS Trace Max 21500MILS



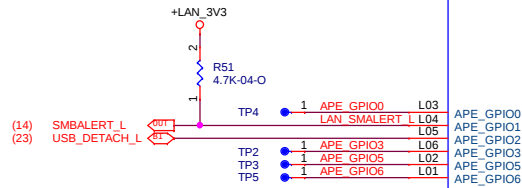
These resistors must be installed with the BCM5761 only.



Ruart_mode should be installed to enable the debug UART function when the BCM5754 is used.



Rd8_pd must be installed with the BCM5761 only.

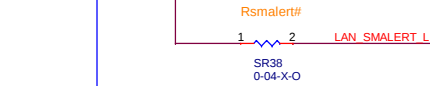
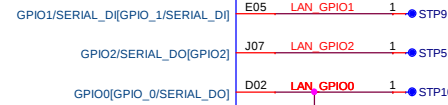
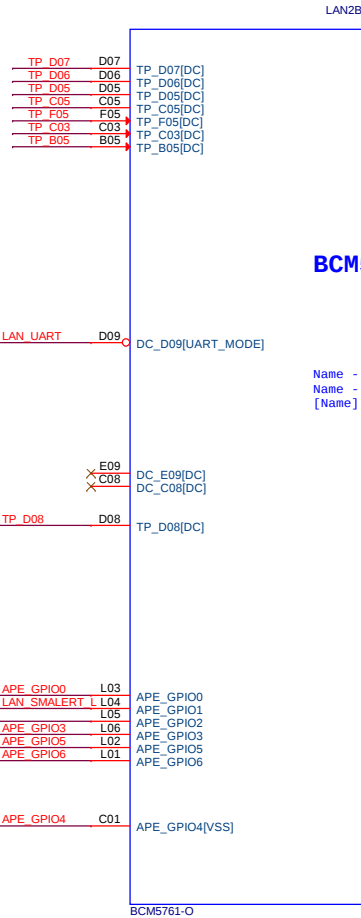


Rvss_5754 must be installed when the BCM5754 is used.

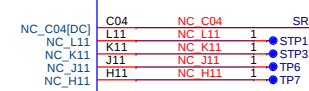


BCM5761/BCM5754

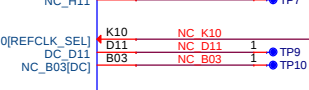
Name - 5761
Name - 5754 unless different
[Name] - 5754 only



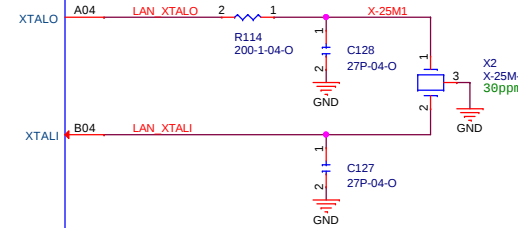
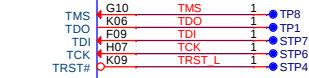
Rsmalert# should be installed when the BCM5754 ASF doorbell function is used.



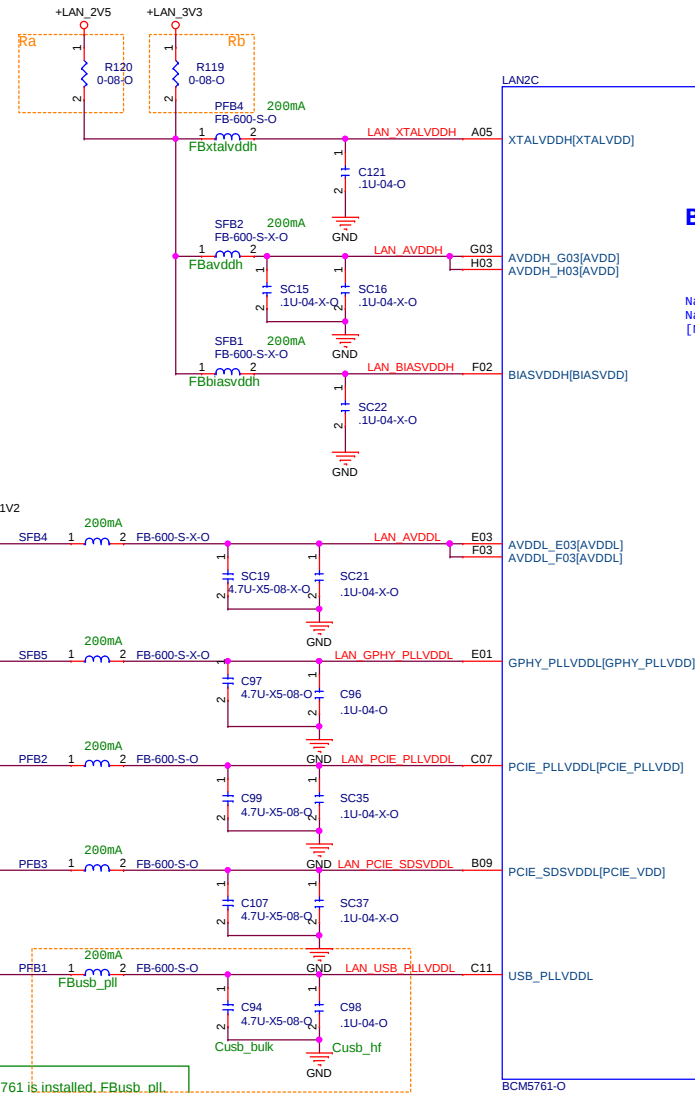
For Energy Detection function use only for 5761E use



Rrefclkssel must not be installed with the BCM5761, but may be installed with the BCM5754

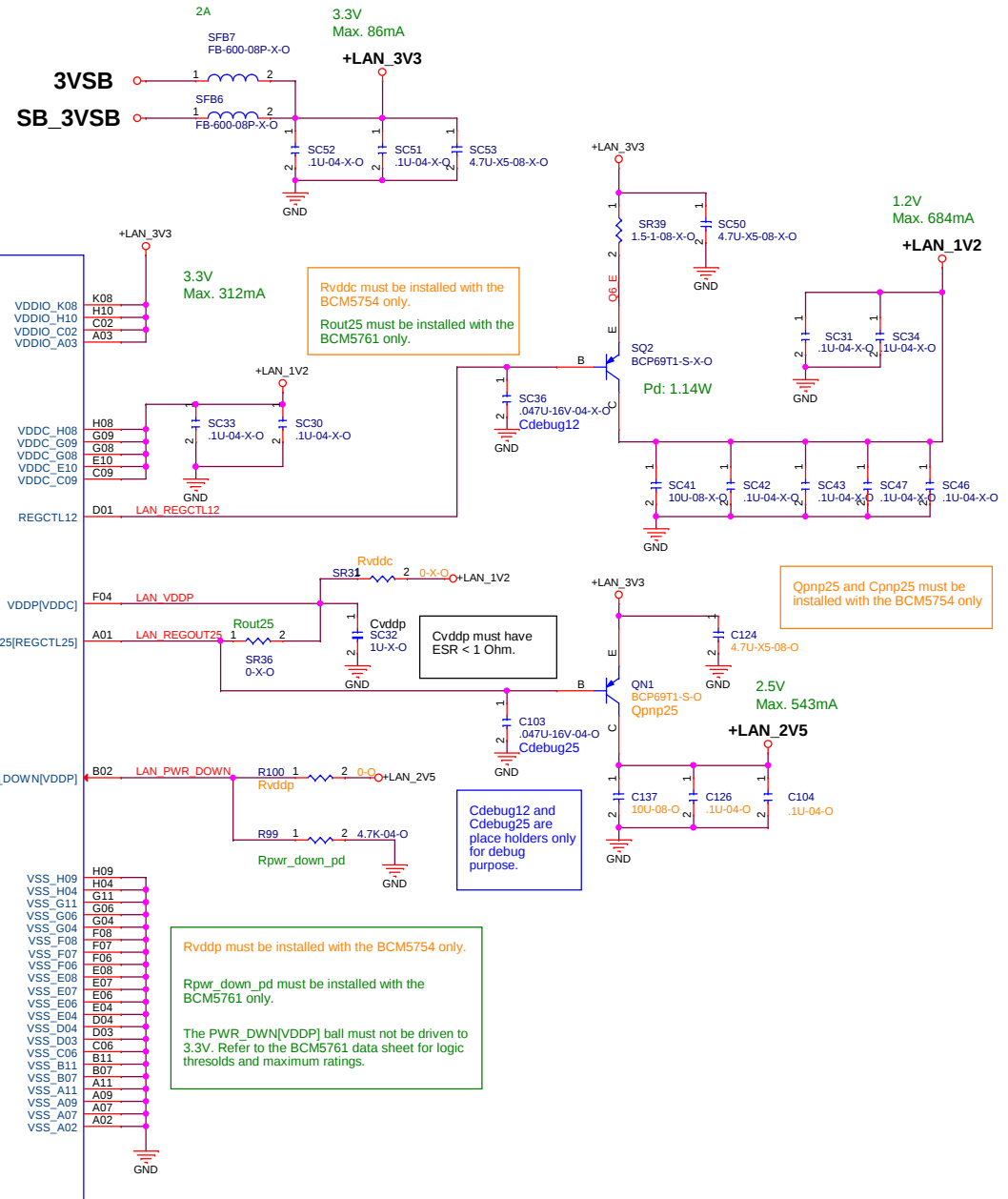


	5754	5761
Ra	V	X
Rb	X	V



BCM5761/BCM5754

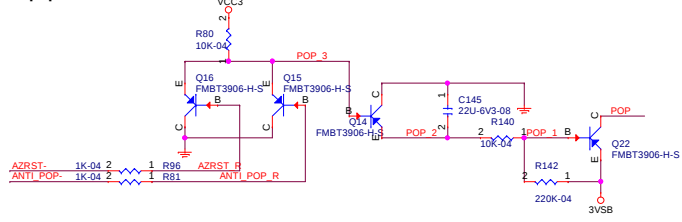
Name - 5761
Name - 5754 unless different
[Name] - 5754 only



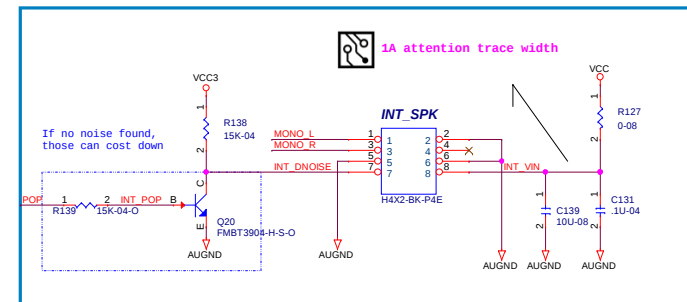
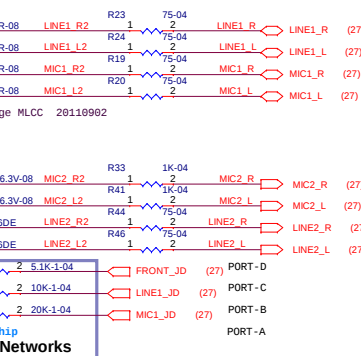
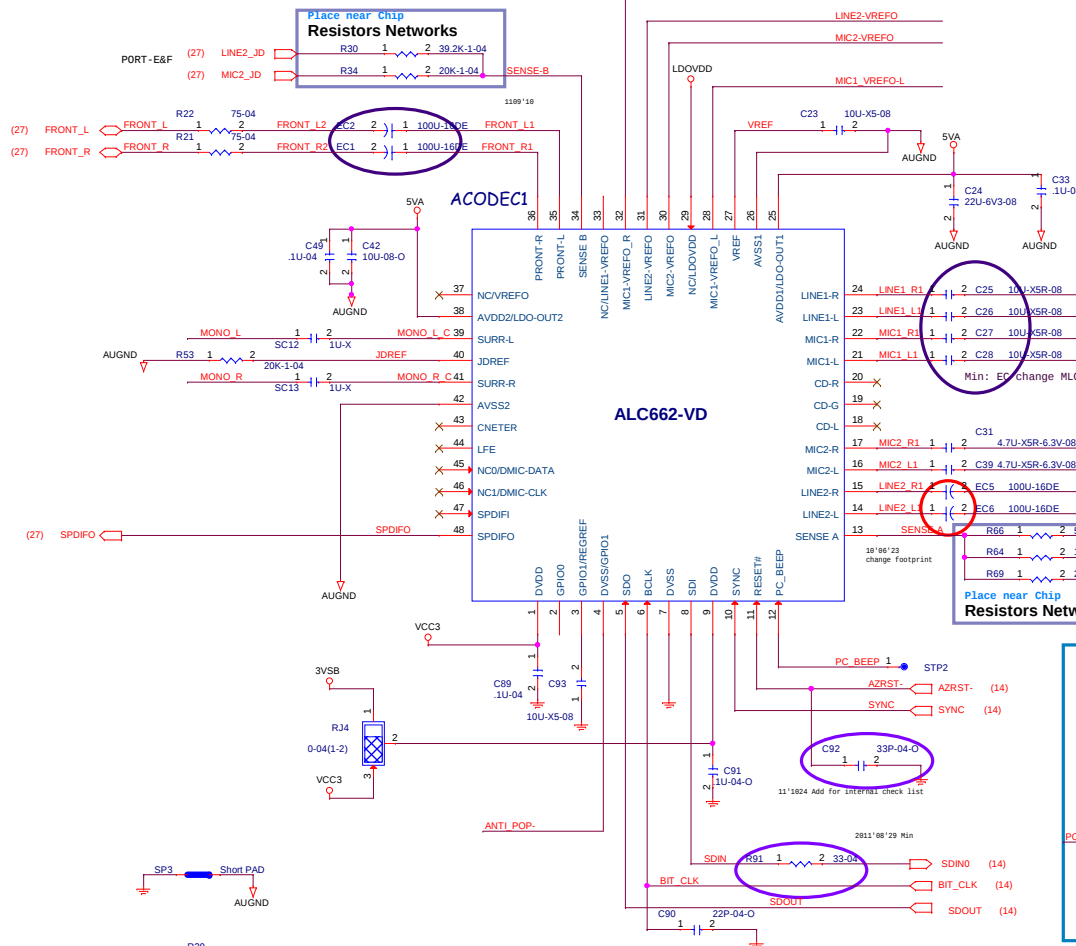
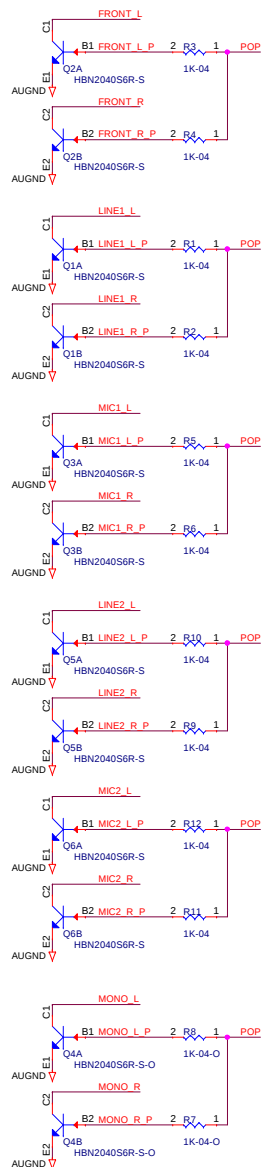
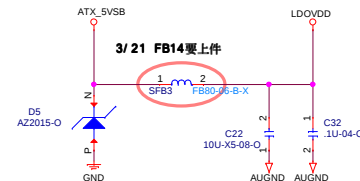
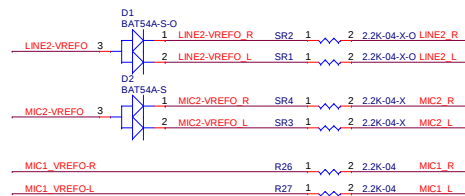
If the BCM5761 is installed, FBusb_pll, Cusb_bulk, and Cusb_hf must be laid out even if the USB interface is not used since the USB PLL may provide an alternate clock source internal to the BCM5761.

If the BCM5754 is installed, FBusb_pll, Cusb_bulk, and Cusb_hf may be uninstalled.

Depop schematic

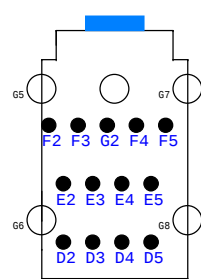
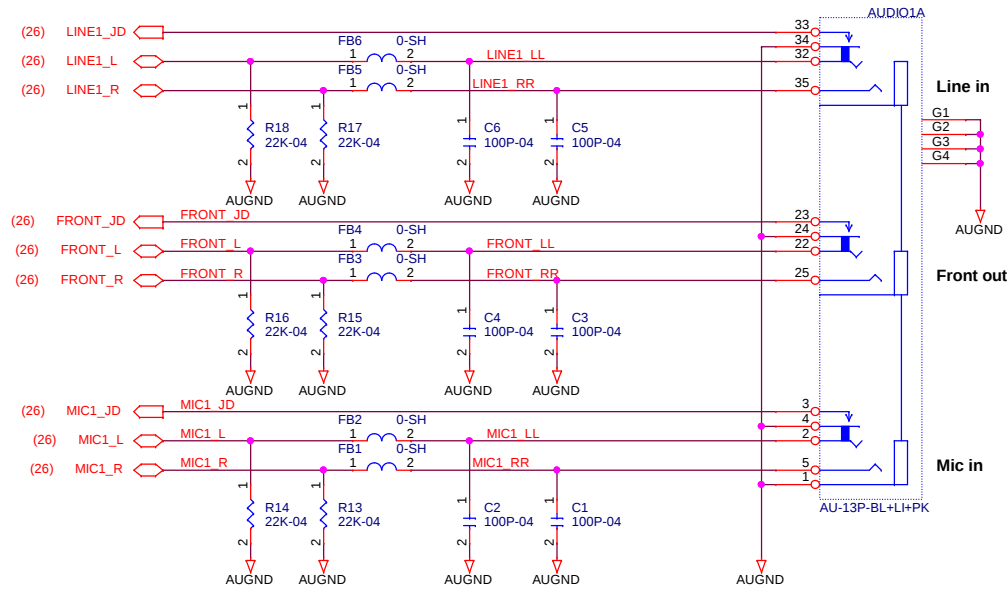


MIC Bias

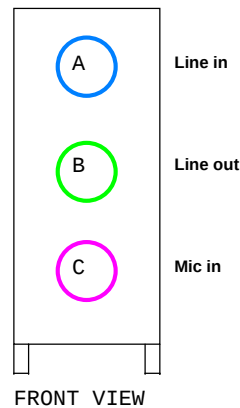


"INTERNAL SPEAKER"
FOR COMMERCIAL AND AIO SERIES USE

REAR-AUDIO

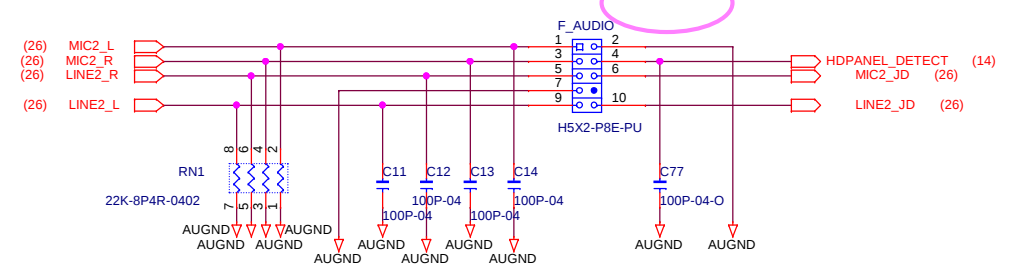


TOP VIEW

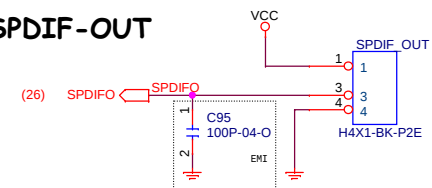


FRONT VIEW

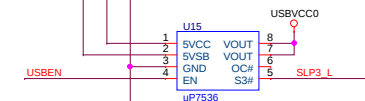
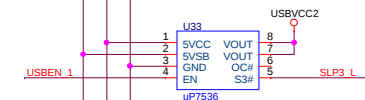
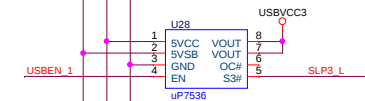
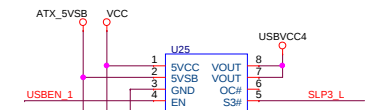
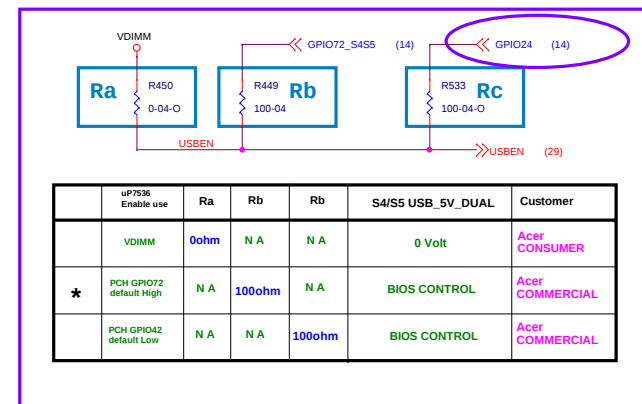
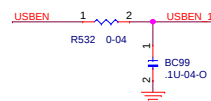
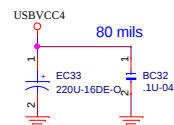
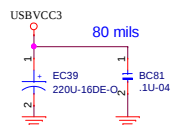
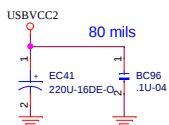
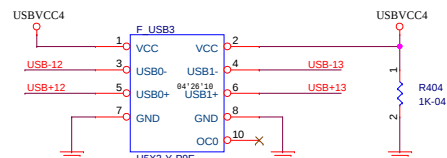
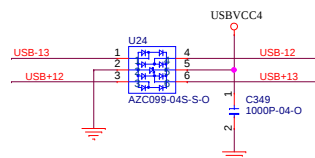
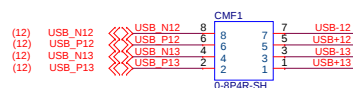
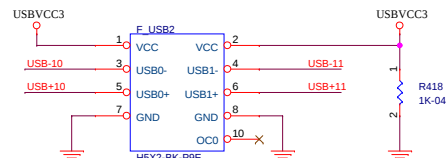
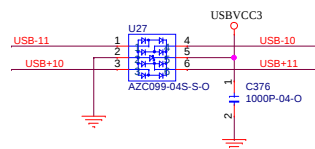
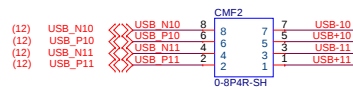
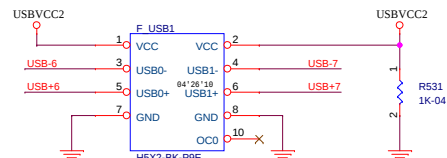
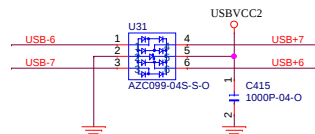
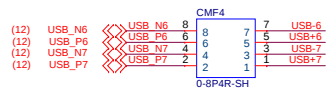
FRONT-AUDIO



SPDIF-OUT

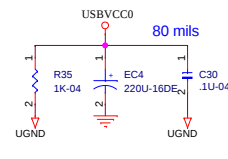
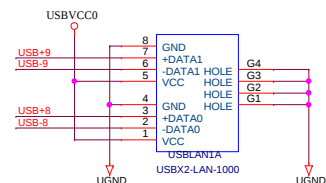
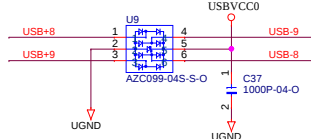
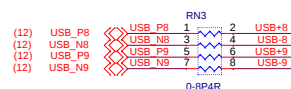


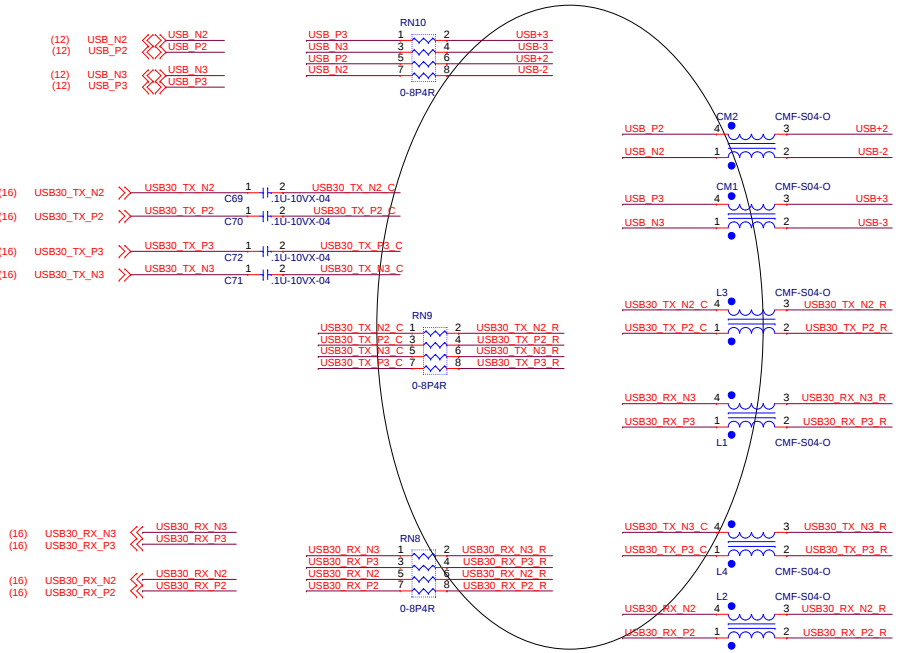
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AUDIO ALC662 Connector (PANEL)			
Size	Document Number	Rev	
B	Q77H2-AD	A	
Date:	Monday, October 31, 2011	Sheet	27 of 49



FRONT PANEL USB2.0 HEADER

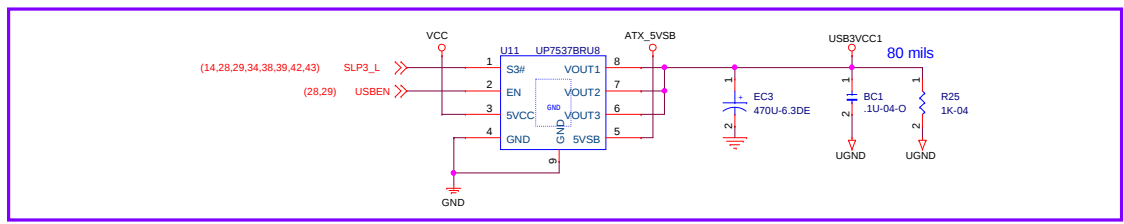
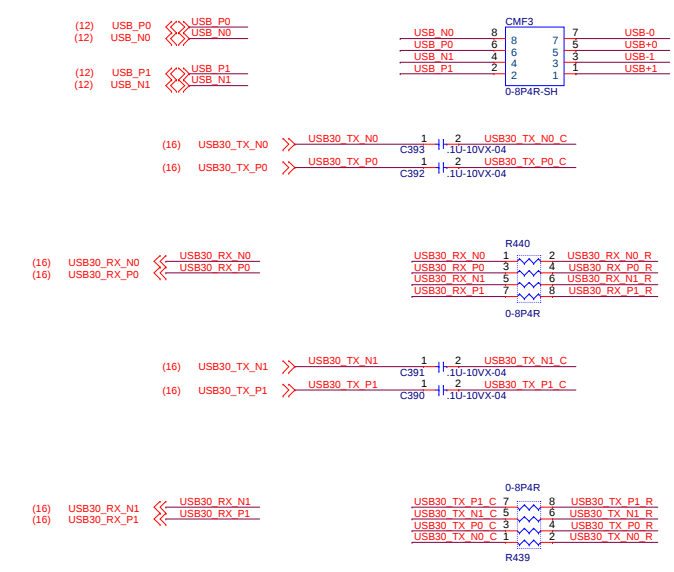
REAR PANEL USB2.0 CONNECTOR



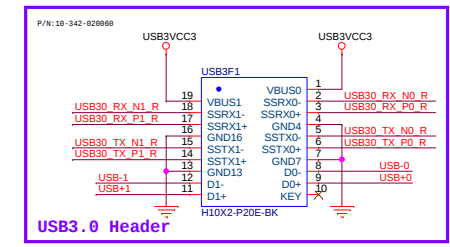
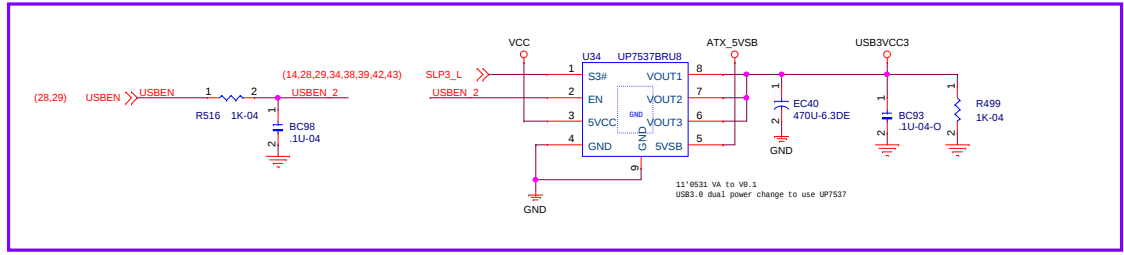
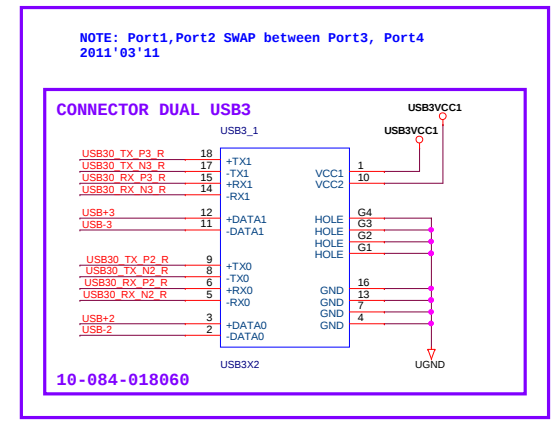
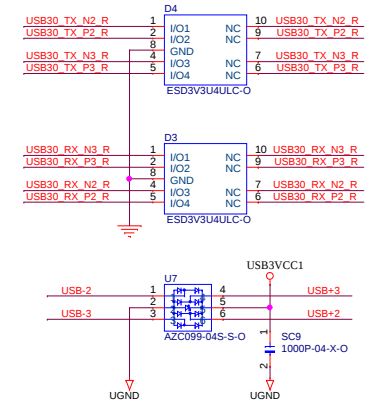


REAR PANEL USB3.0 CONNECTOR

FRONT PANEL USB3.0 HEADER



USB3 ESD COMPONENTS



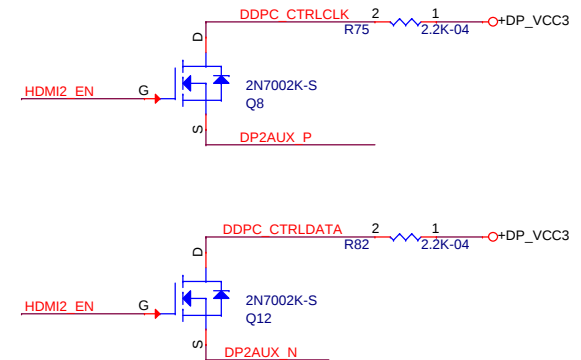
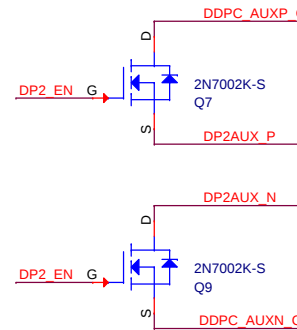
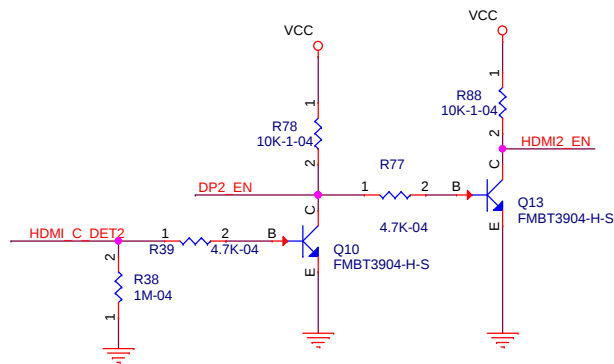
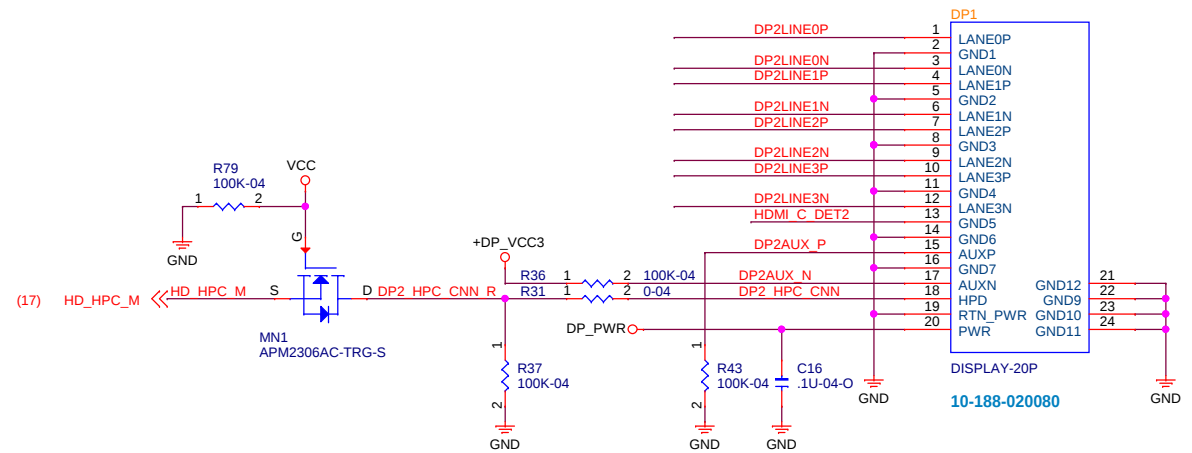
USB3 ESD COMPONENTS

(17) DDPC_CTRLDATA >> DDPC_CTRLDATA
(17) DDPC_CTRLCLK >> DDPC_CTRLCLK

(17) DDPC_AUXP >> DDPC_AUXP C44 1U-10VX-04 DDPC_AUXP C
(17) DDPC_AUXN >> DDPC_AUXN C41 1U-10VX-04 DDPC_AUXN C

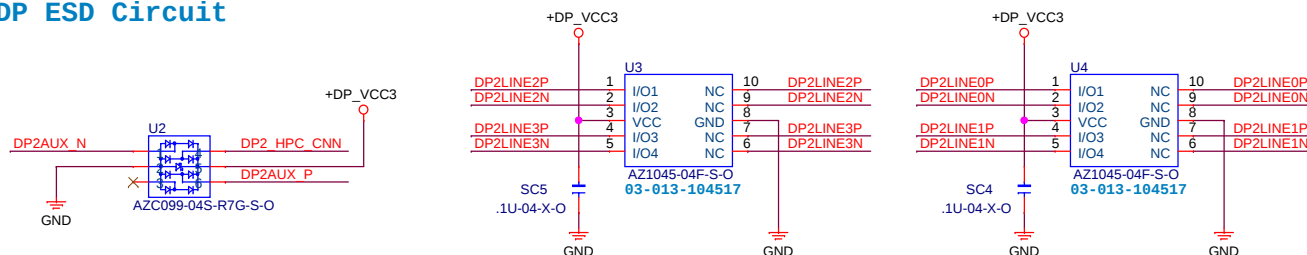
(17) DDPC_0P >> DDPC_0P C53 1U-10VX-04 DP2LINE0P C 8 7 DP2LINE0P
(17) DDPC_0N >> DDPC_0N C54 1U-10VX-04 DP2LINE0N C 6 5 DP2LINE0N
(17) DDPC_1P >> DDPC_1P C55 1U-10VX-04 DP2LINE1P C 4 3 DP2LINE1P
(17) DDPC_1N >> DDPC_1N C56 1U-10VX-04 DP2LINE1N C 2 1 DP2LINE1N

(17) DDPC_2P >> DDPC_2P C57 1U-10VX-04 DP2LINE2P C 8 7 DP2LINE2P
(17) DDPC_2N >> DDPC_2N C58 1U-10VX-04 DP2LINE2N C 6 5 DP2LINE2N
(17) DDPC_3P >> DDPC_3P C59 1U-10VX-04 DP2LINE3P C 4 3 DP2LINE3P
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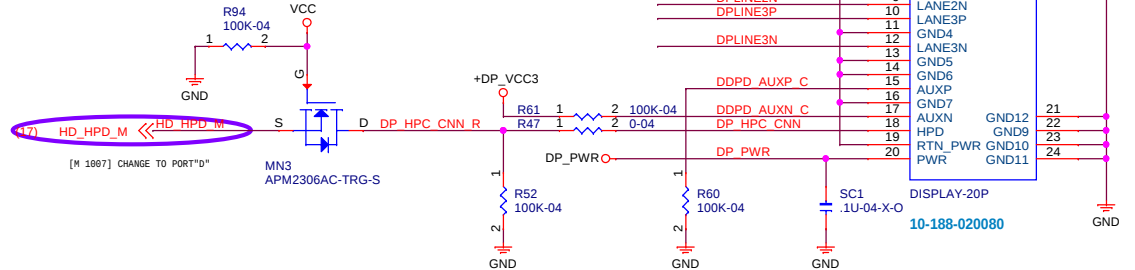
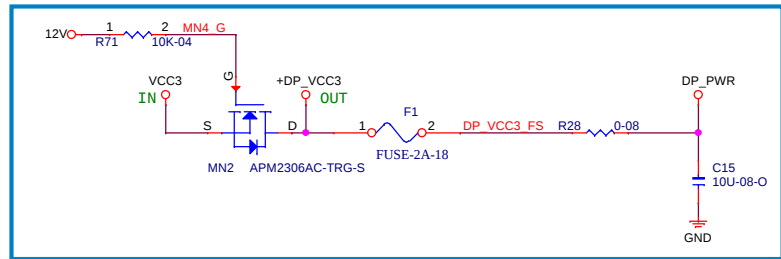
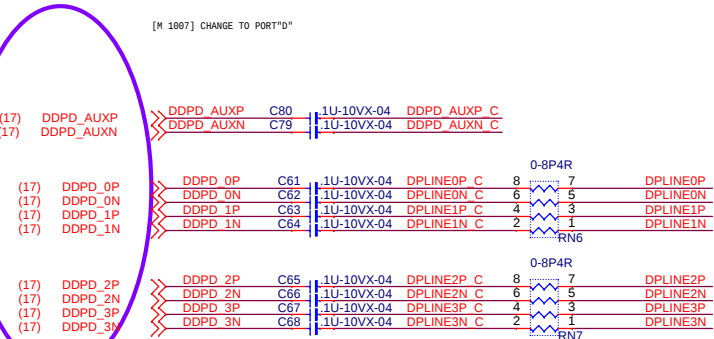


SUPPORT DP TO HDMI/DVI DONGLE

DP ESD Circuit

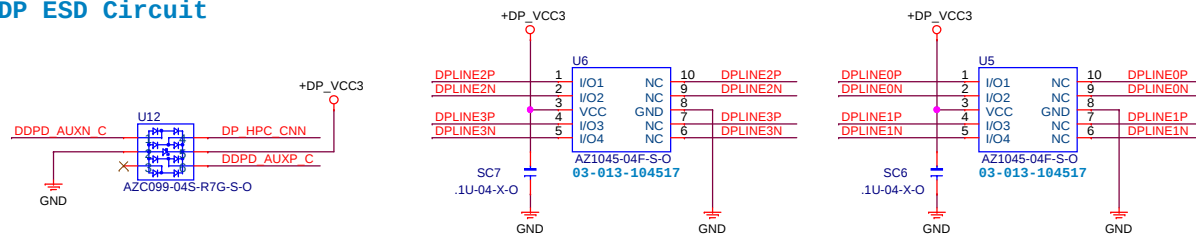


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Size: Custom	Document Number: Q77H2-AD
Date: Monday, October 31, 2011	Sheet: 30 of 49

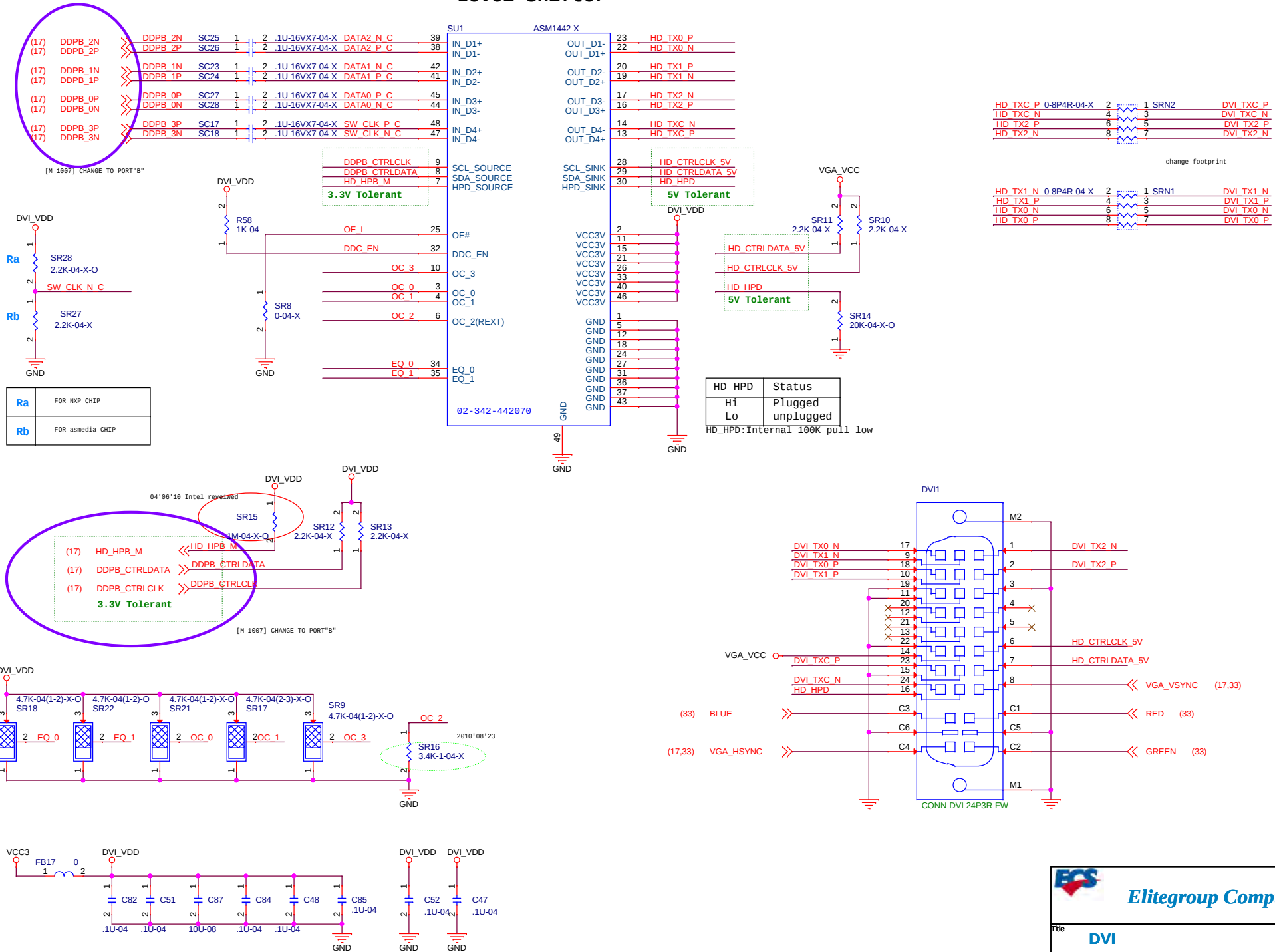


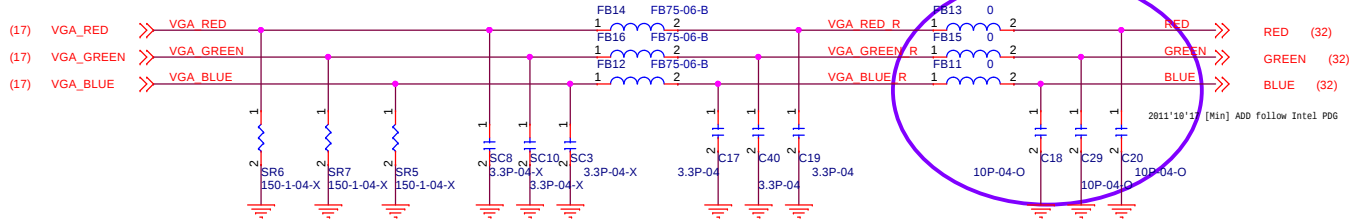
SUPPORT DP TO HDMI/DVI DONGLE

DP ESD Circuit

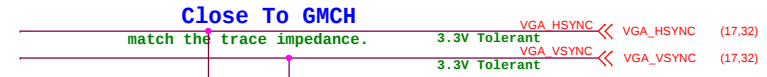


Level Shifter





Close to Connector

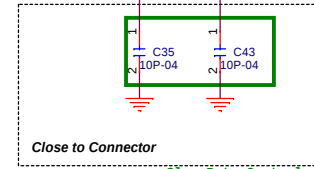


Close To GMCH

match the trace impedance.

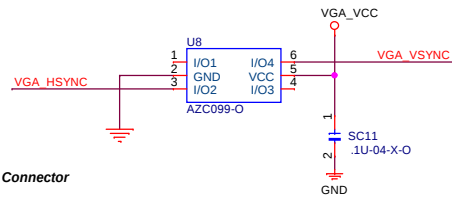
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VGA_VSYNC << VGA_VSYNC (17,32)

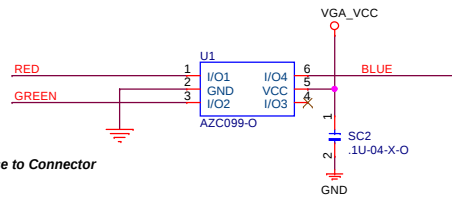


Close to Connector

Slew Rate Control

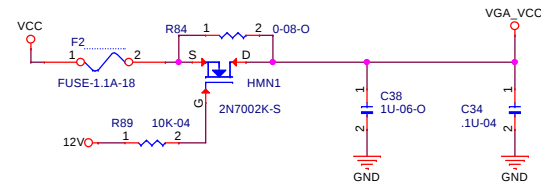


Close to Connector



Close to Connector

If build in Internal DVI/HDMI Con,
that can use the circuit to protect reverse voltage together.



Elitegroup Computer Systems

File
VGA CONNECTOR

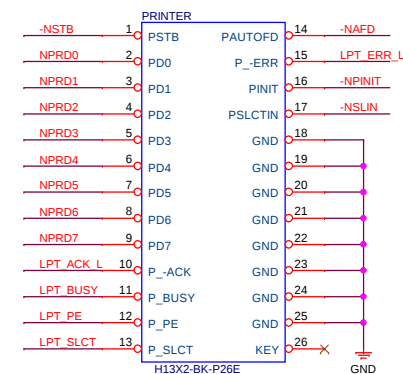
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Date: Monday, October 31, 2011

Document Number
Q77H2-AD

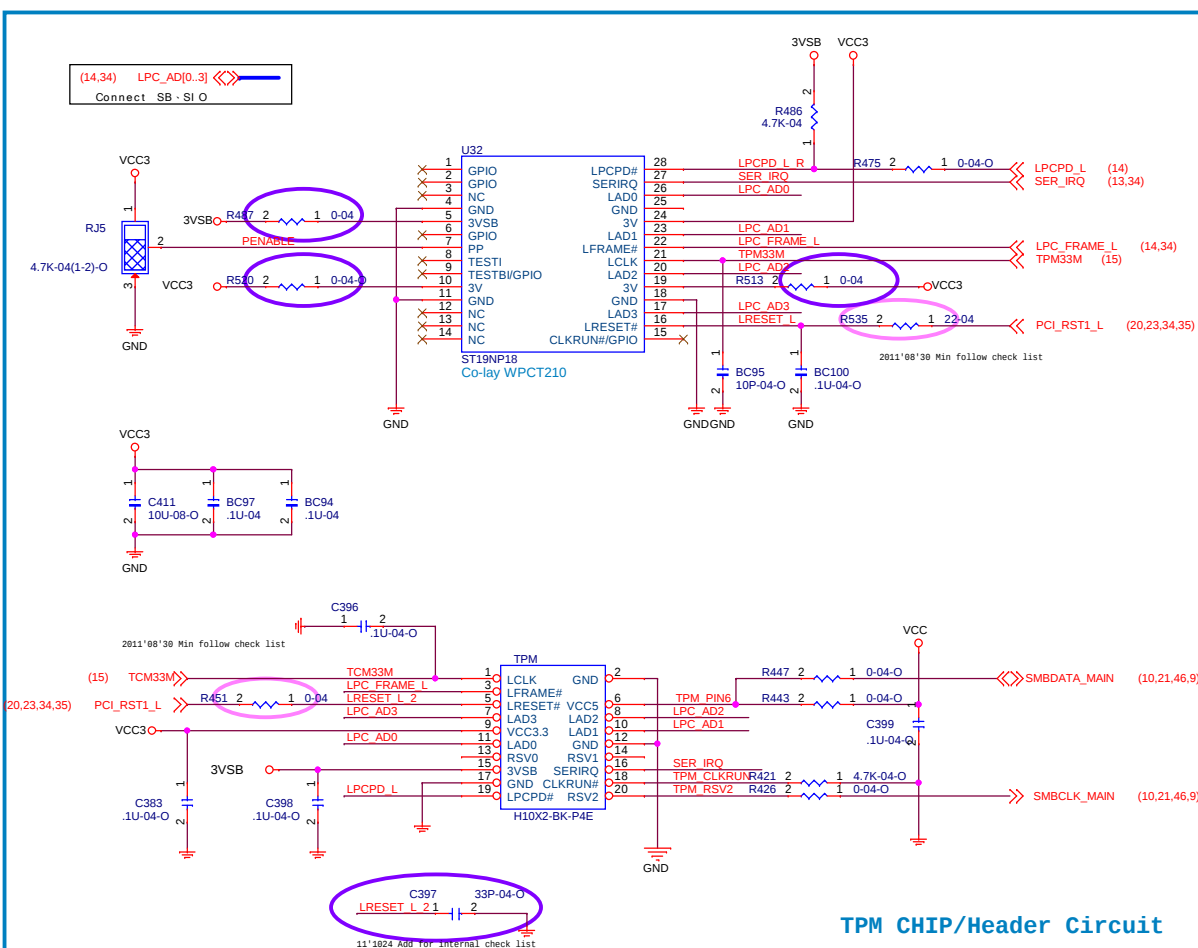
Rev
A

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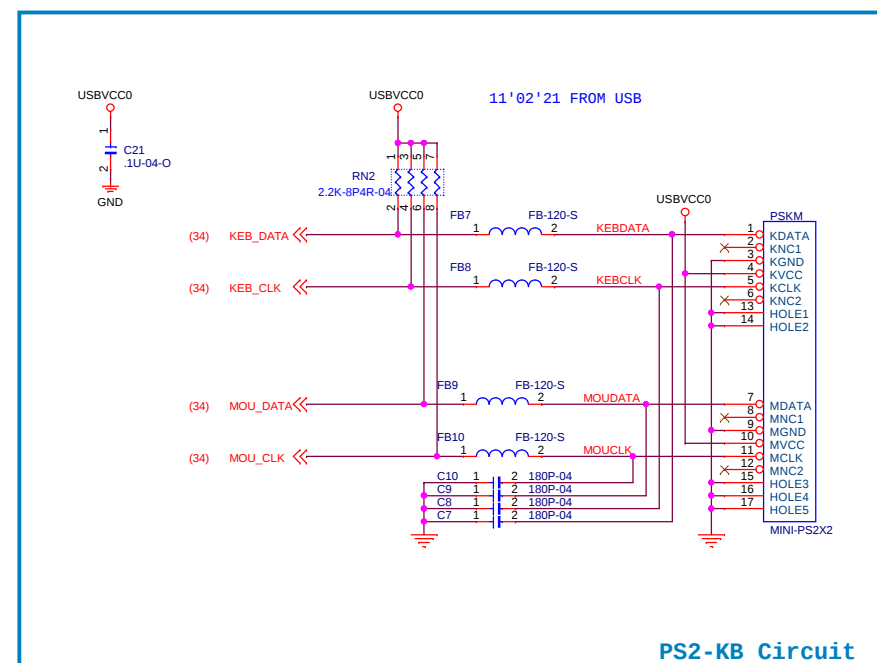


0901 CHANGE FOR RFQ

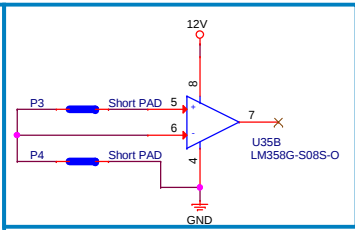
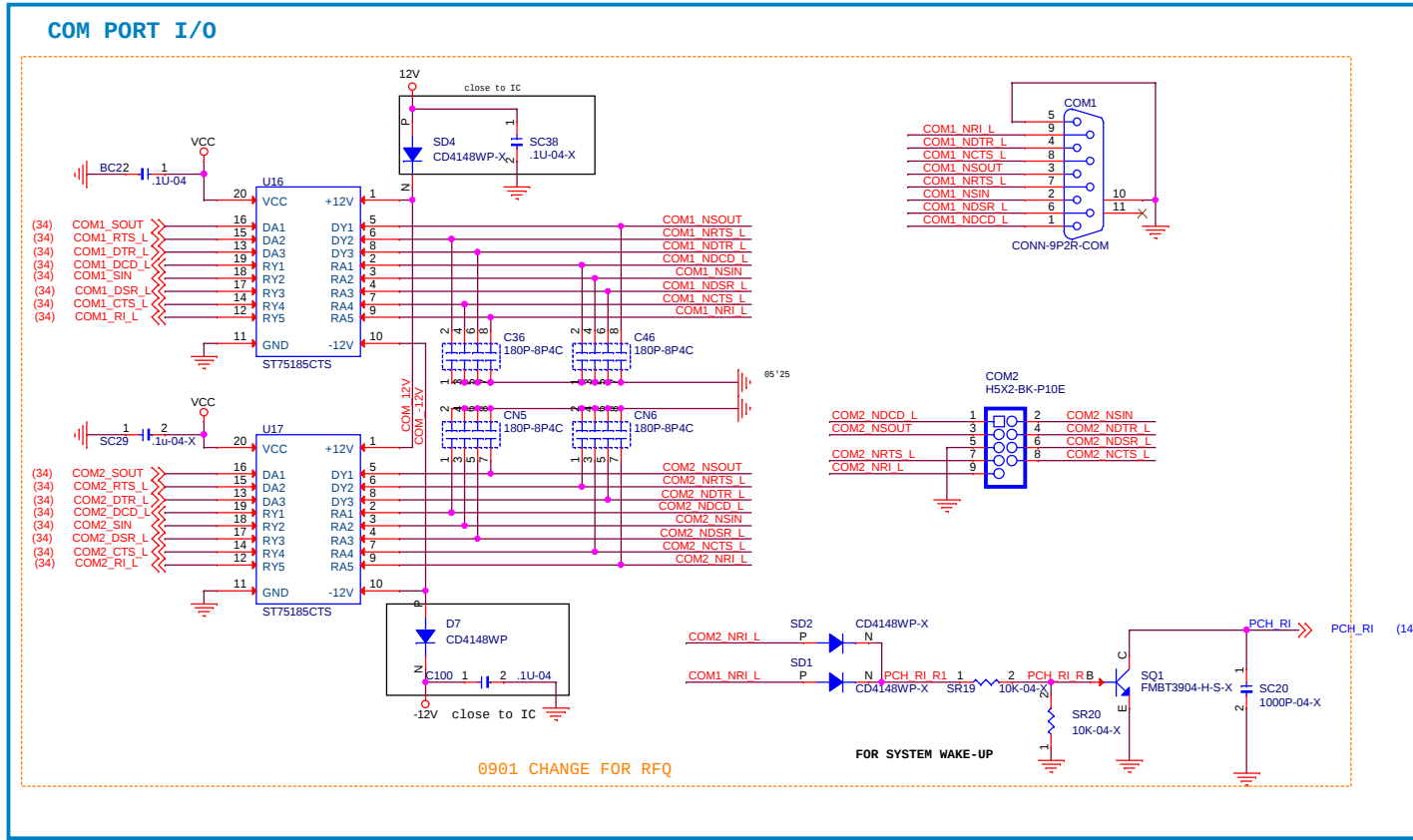
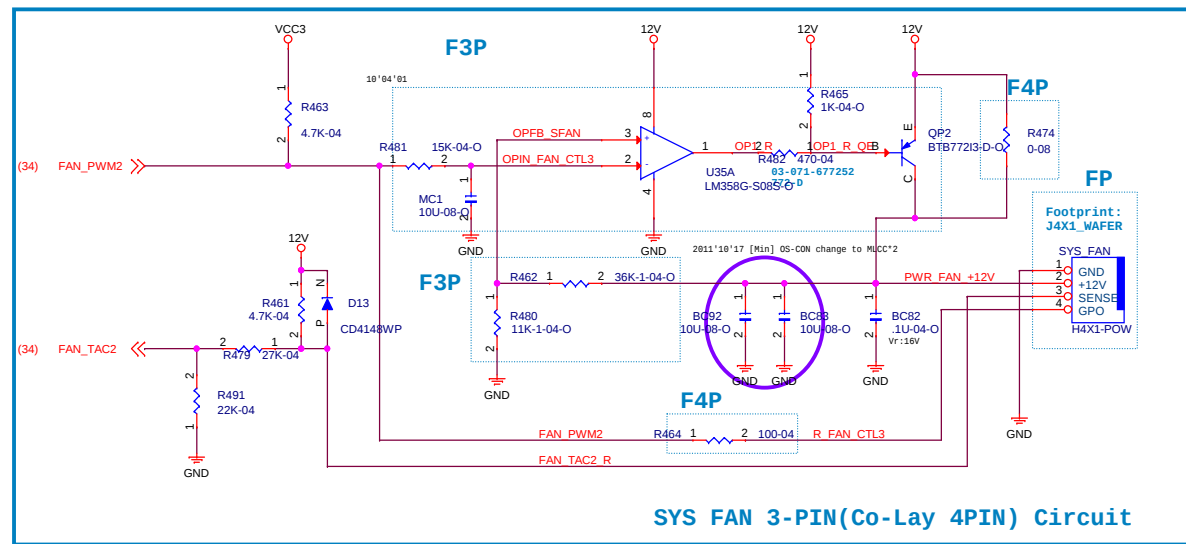
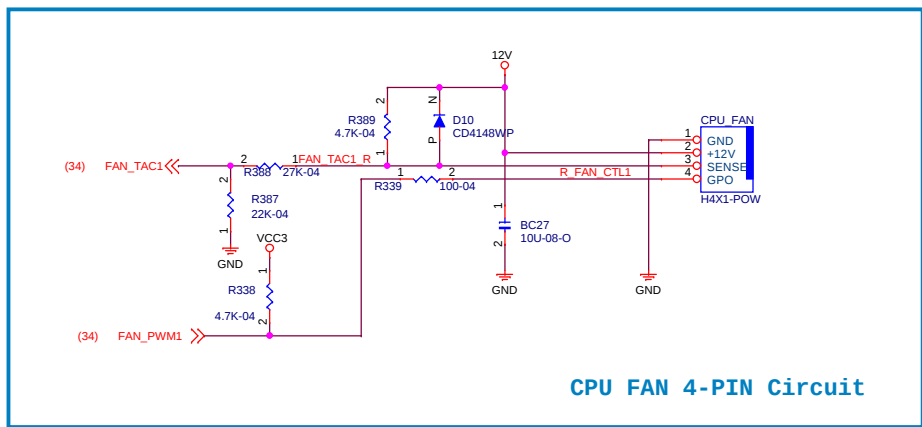
LPT Header Circuit



TPM CHIP/Header Circuit



PS2-KB Circuit

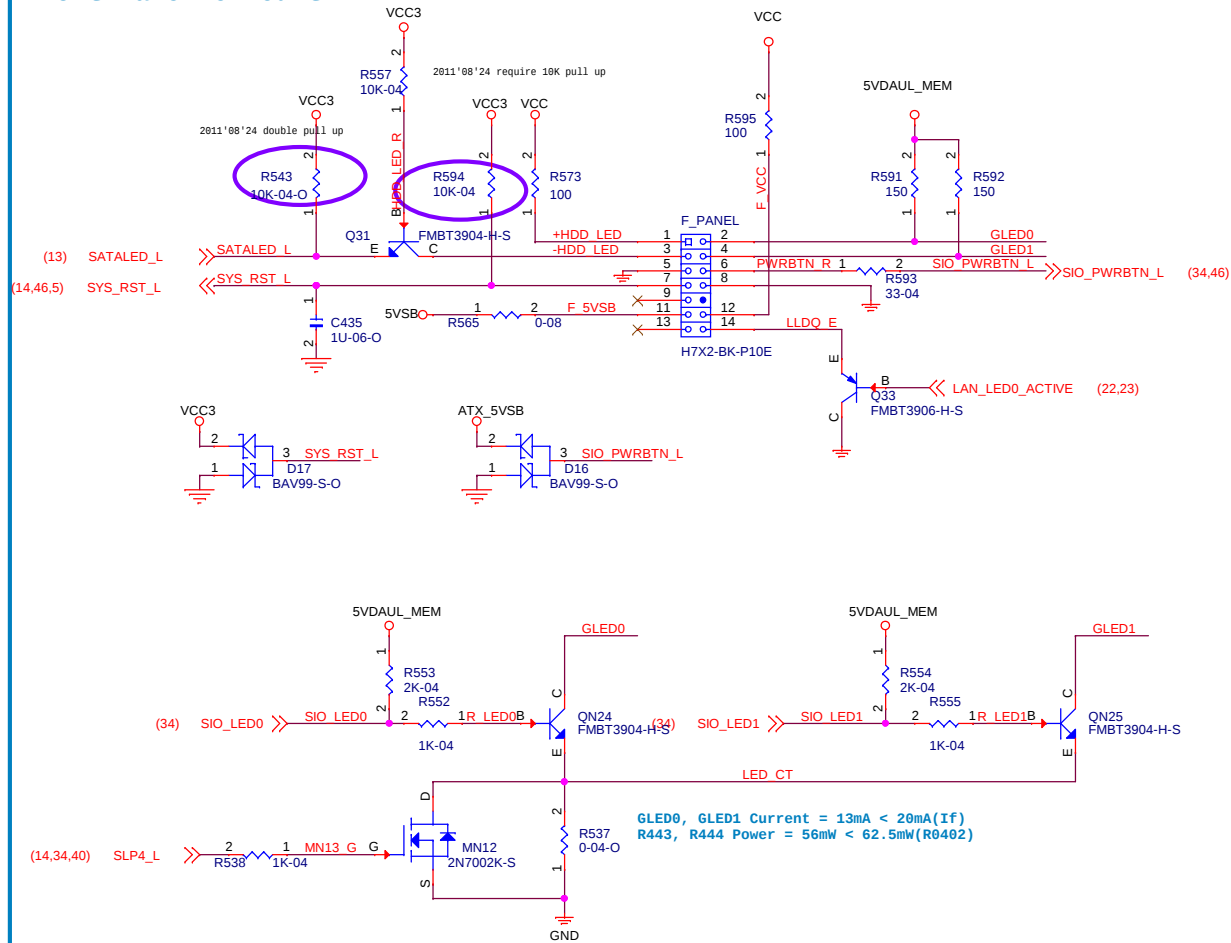


MODE	F3P	F4P	FP Value
* 3PIN	V	X	H3X1-P-W
4PIN	X	V	H4X1-P-W

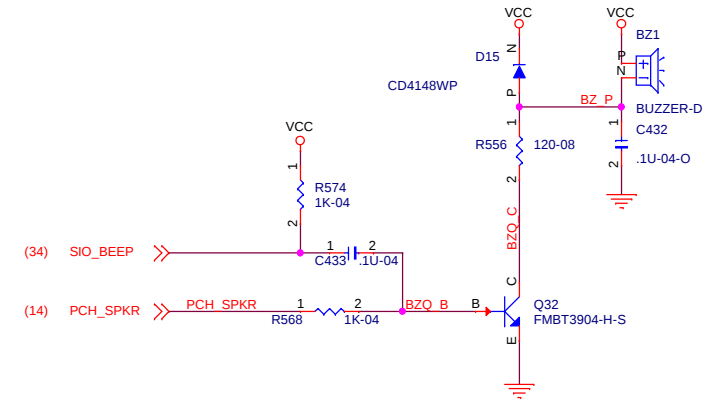
0901 CHANGE FOR RFQ

+ - terminal add short pad to ground for nonuse OP , 20110406

Front Panel Circuit



Buzzer Circuit



Elitegroup Computer Systems

Title		
F_PANEL, BUZ		
Size	Document Number	Rev
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MODIFY Ra/Rb VALUE FOR FOLLOWING RULES

- 1)AC ON: 3VSB vs RSMRST(t_{204} : min 10ms)
- 2)AC OFF: 3VSB>2.9V when RSMRST<0.8V



FOR COSTDOWN

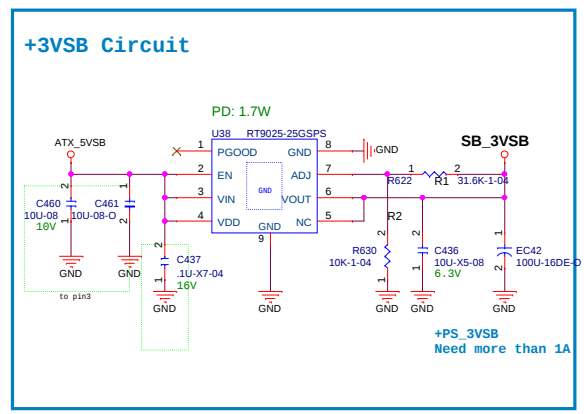
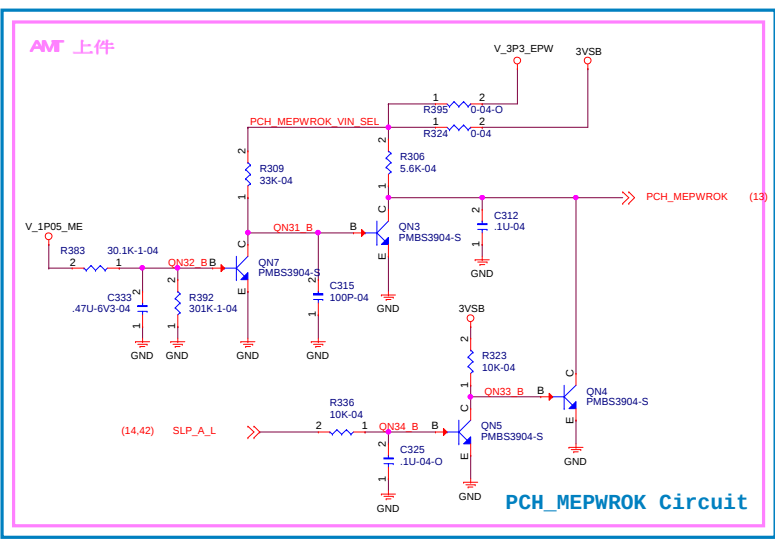
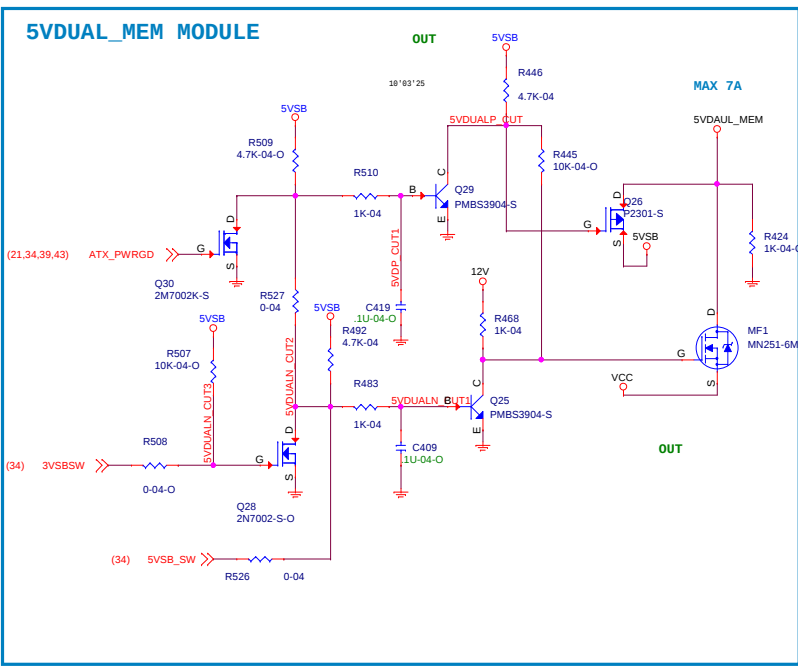
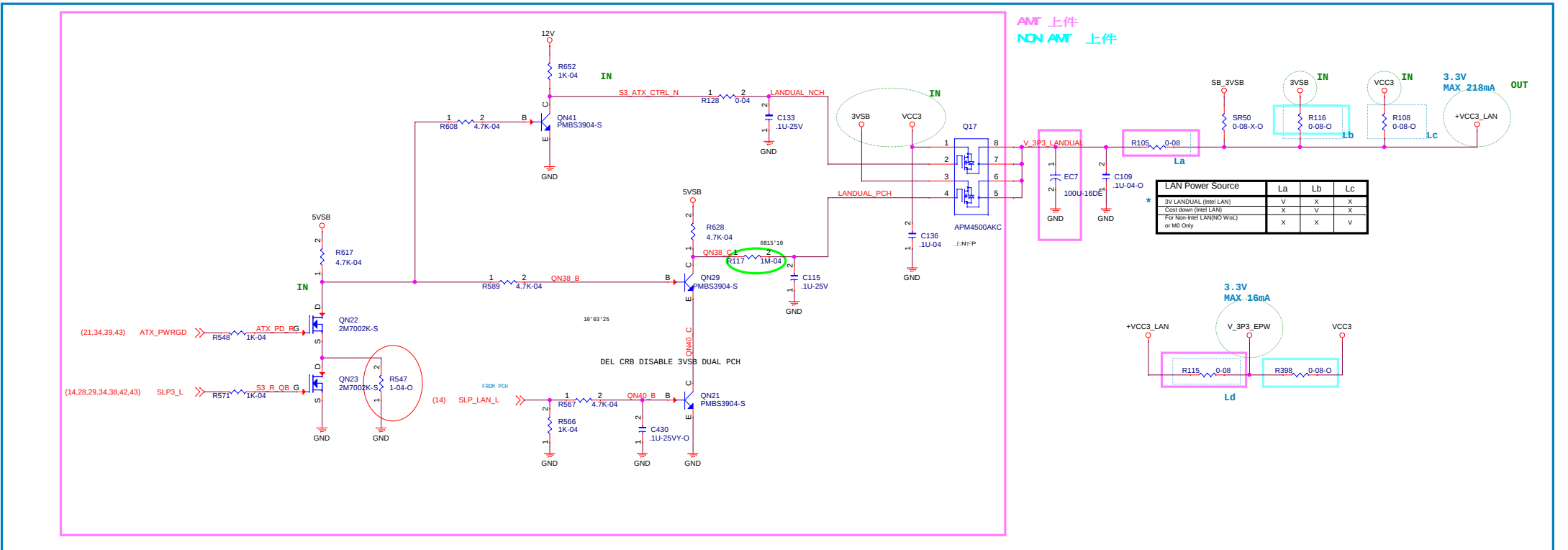


R598 0.04 FOR COSTDOWN



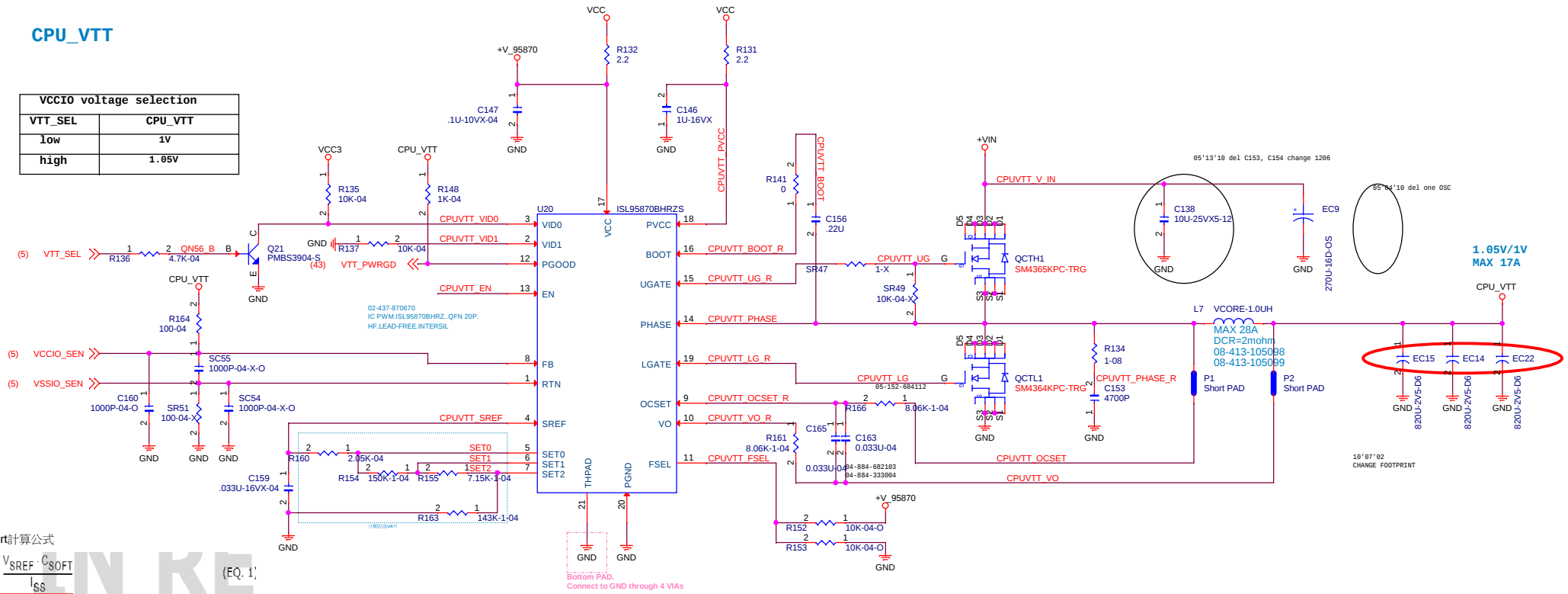
(14,46,5





CPU_VTT

VCCIO voltage selection	
VTT_SEL	CPU_VTT
low	1V
high	1.05V



Soft-start計算公式

$$t_{SS} = \frac{V_{SREF} \cdot C_{SOFT}}{I_{SS}} \quad (EQ. 1)$$

Where:

- I_{SS} is the soft-start current source at the 20μA limit
- V_{SREF} is the buffered V_{REF} reference voltage

Vout計算公式

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT			
VID1	VID0	CLOSE	V _{SREF}	V _{OUT}	
1	1	SW0	V _{SET1}	V _{OUT1}	
1	0	SW1	V _{SET2}	V _{OUT2}	
0	1	SW2	V _{SET3}	V _{OUT3}	
0	0	SW3	V _{SET4}	V _{OUT4}	

Equations 21, 22, 23 and 24 give the specific V_{SET} equations for the ISL95870B setpoint reference voltages.

The ISL95870B V_{SET1} setpoint is written as Equation 21:
 $V_{SET1} = V_{REF}$ (EQ. 21)

The ISL95870B V_{SET2} setpoint is written as Equation 22:
 $V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}}\right)$ (EQ. 22)

The ISL95870B V_{SET3} setpoint is written as Equation 23:
 $V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}}\right)$ (EQ. 23)

The ISL95870B V_{SET4} setpoint is written as Equation 24:
 $V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}}\right)$ (EQ. 24)

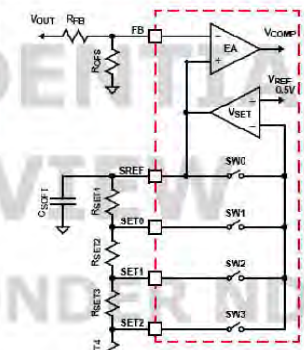
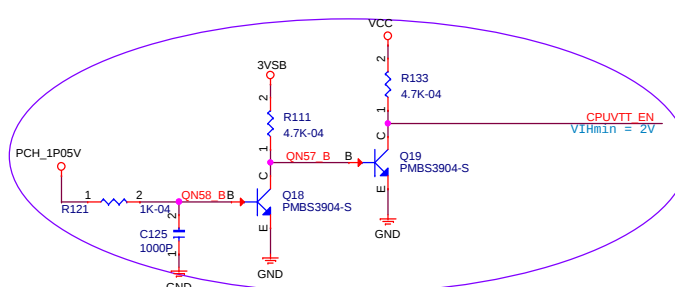
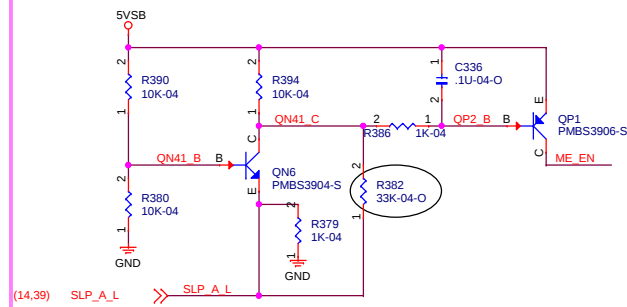


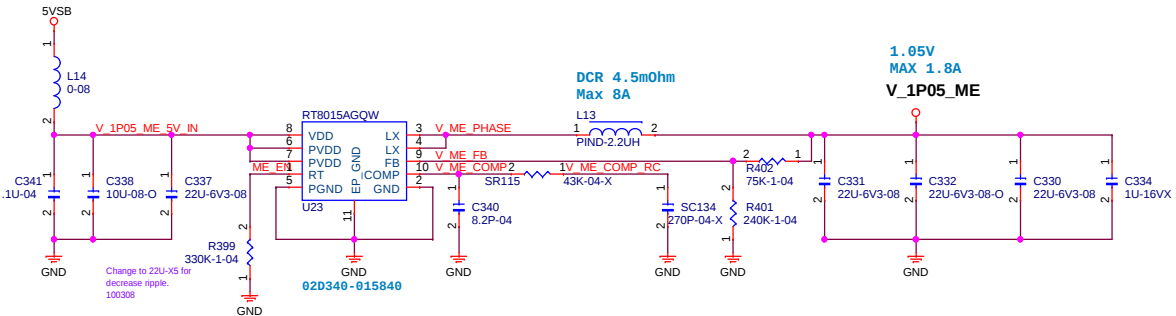
FIGURE 10. ISL95870B VOLTAGE PROGRAMMING CIRCUIT

Frequency selection	
F(Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC





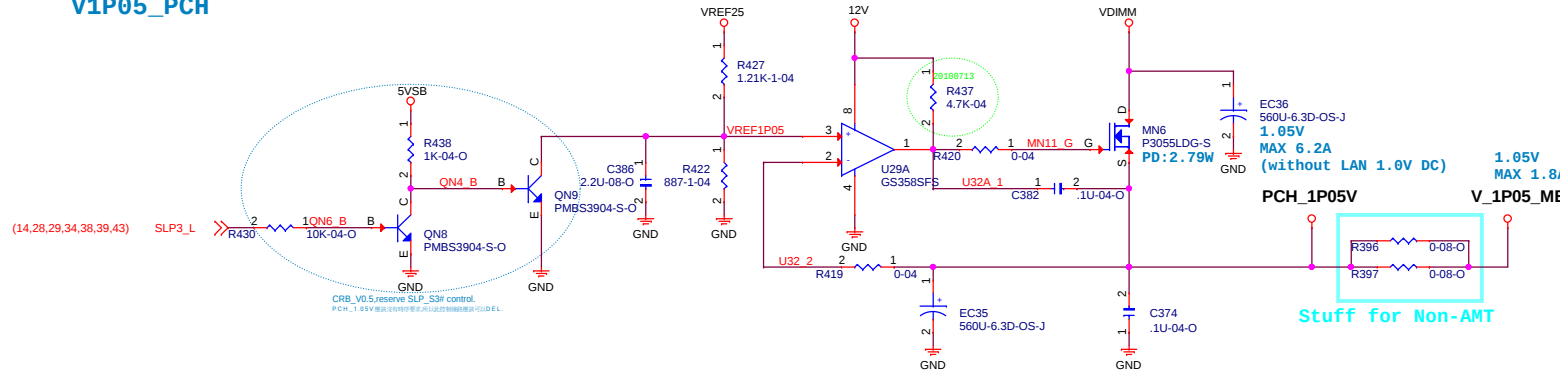
SLPAMT_L	EN	V_1P05_ME
High	5VSB	Enable
Low	0 V	Disable



V1P05_ME

AMT 上件

V1P05_PCH

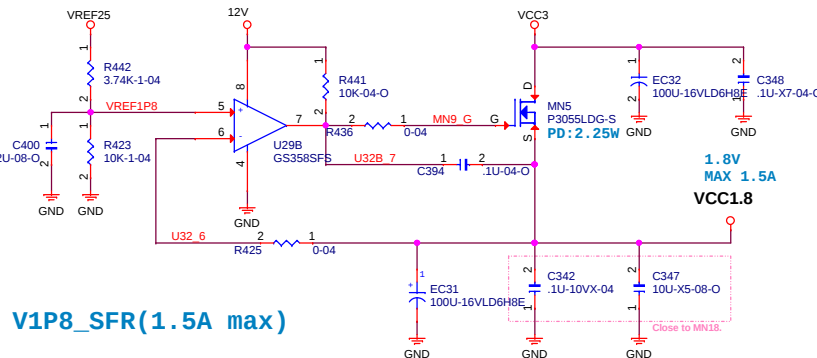
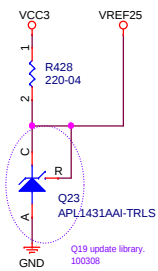


BOM Note:

- 02-340-015840...dnt10_r8106a
IC REG.RT8015AGQW.WDFN 10P.3A LEAD-FREE(RoHS/HF).
RICHTEK
- 08-413-225094...choke_2r2m_p4d9x4d6mm
POWER IND 2.2uH 20% 8A 4.5m OHM DIP 29 8.2x9.2x7.5x6.7
mm AKL0806MN-2R2W-13.2...LEAD-FREE(RoHS) MAGIC
- 05-152-750113
RES 75K 1/16W 1% SMD 0402...LEAD-FREE(RoHS/HF).
- 05-152-430103
RES 43K 1/16W 5% SMD 0402...LEAD-FREE(RoHS/HF).
- 05-152-240114
RES 240K 1/16W 1% SMD 0402...LEAD-FREE(RoHS/HF).
- 04-890-829100
C/C 8.2pF 50V 0.25pF...SMD 0402...LEAD-FREE(RoHS/HF).

Stuff for Non-AMT

VREF25



V1P8_SFR(1.5A max)

Elitegroup Computer Systems

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★

Stuff VSAGz

VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

*

VCCSA voltage selection	
Rf	+V_SA
unstuff	0.85V
stuff	0.925V

VCCSA voltage selection	
Rf	+V_SA
unstuff	0.85V
stuff	0.925V



OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5(CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0

OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5(CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0

CSA Sequence

The diagram illustrates the CSA Sequence circuit, which consists of two identical stages. The top stage is driven by the VTT_PWRGD signal (pin 41) through a 10K-04 resistor (R484) to the base of the NPN transistor QN13 (PMBS3904-S). The bottom stage is driven by the SLP3_L signal (pins 14, 28, 29, 34, 38, 39, 42) through a 10K-04 resistor (R523) to the base of the NPN transistor QN14 (PMBS3904-S). Both stages have a 5VSB supply connected to the base through a 10K-04 resistor (R521 for the top stage, R522 for the bottom stage). The emitters of all transistors are connected to GND. The collectors of QN13 and QN14 are connected to the VCCSA_COMP signal line. The output of the top stage is also connected to the base of QN10 (PMBS3904-S), and the output of the bottom stage is connected to the base of QN11 (PMBS3904-S). The emitters of QN10 and QN11 are connected to GND, and their collectors are connected to the VCCSA_COMP signal line.

